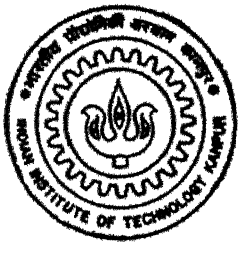
KANSYS: A CAD TOOL FOR ANALOG CIRCUIT SYNTHESIS

by

SANDEEP KUMAR GUPTA



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

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KANSYS: A CAD TOOL FOR ANALOG CIRCUIT SYNTHESIS

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SANDEEP KUMAR GUPTA

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INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

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Dedicated to
My Parents

Certificate

This is to certify that the work contained in this thesis, entitled *KANSYS: A CAD TOOL FOR ANALOG CIRCUIT SYNTHESIS* , has been carried out by *SANDEEP KUMAR GUPTA* under my supervision and that this work has not been submitted elsewhere for a degree.

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Abstract

A CAD tool for the synthesis of analog circuits from element level (say a transistor) to a macrocell (say an active filter) has been developed. A top-down knowledge intensive, hierarchically structured framework is adopted which demonstrates the feasibility of attacking tightly coupled analog design problems in a highly stylized, hierarchical fashion. Exploiting hierarchy permits the design process to be recast as a sequence of smaller design tasks, alternating between design style selection and translation, and permits the sub blocks to be reused in different contexts. A flattened view of the design is not, however, lost sight of and some of the design tricks that jump across many levels of hierarchy are used. KANSYS synthesizes sized transistor schematics for CMOS OPAMPs from performance and process specifications. Detailed circuit simulation demonstrates that KANSYS is capable of synthesizing functional circuits.

Acknowledgement

I express my deep sense of gratitude to my thesis supervisor, Dr. M. M. Hasan, for giving me valuable guidance and encouragement during this work.

I thank all of my friends who have made my stay here a memorable one.

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INTRODUCTION

While sophisticated CAD techniques have been developed to automate the design of digital circuitry, the progress towards automating the analog circuit design task started towards the end of the last decade. Analog circuitry is widely used in system applications such as telecommunications and robotics, where analog interfaces to an external environment are coupled with DSP systems. For a mixed analog digital ASIC design on which 90 percent of the devices are used in digital circuitry and only 10 percent of the devices are used in analog circuitry, analog circuit design task might well be the limiting factor in the overall design time. Because of the sensitive economic environment for ASIC designs, any delay is extremely expensive due to the loss of potential sales. Therefore there is a strong economic need for improved CAD tools to support analog circuit design.

The work of the human analog circuit designer can be arbitrarily divided into three phases:

1. Creating analytical expressions("equations") for the behaviour of new circuit topologies and creating appropriately simplified device and circuit models.

2. Using analytical expressions to guide the selection of both an appropriate combination of circuit topologies and a set of device parameters which together will cause the whole system to meet its performance specifications.

3. Designing the mask geometries from sized transistor level schematics.

In this work, we try to attempt only phase 2 : using analytical expressions to develop sized transistor level schematics to meet performance specifications.

Some ideas from digital design methodologies such as standard cell libraries and module generators have been applied to analog design task. However such techniques have several drawbacks e.g. libraries allow the designer to make only crude tradeoffs among performance specifications and they become obsolete rapidly in the face of technology evolution.

In this work, the framework is knowledge intensive in that it relies heavily on the codification of mature analog design expertise. This knowledge is applied to hierarchically designed circuits. However expert designers often apply design tricks that jump across many levels of hierarchy to achieve better performance. To incorporate some of these, a "flattened" view of the circuit is retained. Since the analytical expressions that we use are in most of the cases limited to first order effects, this approach in fact turns out to be necessary.

OUTLINE OF THE THESIS

Chapter 2 contrasts analog and digital domains of design, discusses equation based design strategy, and summarizes related research.

Chapter 3 describes in detail the architecture and implementation of KANSYS(Kanpur ANalog SYnthesiS) synthesis framework. We describe methods to exploit analog design knowledge and consider how the analog design knowledge is codified within KANSYS.

Chapter 4 considers a few design examples to illustrate our strategy.

Chapter 5 presents the results – synthesized circuits for some sets of specifications

- and the performance evaluation.

Chapter 6 presents some concluding remarks and the scope for future work.

Chapter 2

BACKGROUND

The two approaches to tools for analog synthesis are bottom up layout based approaches and top down knowledge based approaches [1]. Out of these, the first one shows the direct influence of digital ideas. Semi custom analog styles, such as transistor arrays and analog standard cells provide a rapid path to silicon for analog functions already designed to the level of the primitive devices available in the layout style.

Transistor arrays provide the most design flexibility since they provide a small set of atomic primitives from which many circuits can be built. However the layout density is poor as compared to the standard cell approach. Standard cells, on the other hand, lack in design flexibility since the designer is restricted to the library of fixed circuit blocks. Both approaches constrain the circuit design itself: device parameters are not continuously variable because only a limited set of device/circuit types is available. Above all, the nature of the performance specifications of an analog block, quite different from that of a digital block, make storing sufficient designs to span a significant portion of the designable space impossible e.g. the operational amplifier design described takes 13 specifications (including both the performance and the process specifications) each of which is a continuous variable : thus the design space is thirteen dimensional. To simply make 3 values (low,medium

and high) available for each performance specification would require a library with almost **1.5 million** operational amplifier designs.

A higher level approach is the use of analog module generator. These fix some portions of circuit's topology and parametrize the remainder into a limited number of devices. Regular structures, such as switched capacitor filters are particularly amenable to this approach. Some systems, such as AIDE2, use both approaches incorporating standard cells as subunits of a module generator. However these approaches still leave much to be desired : frequently most of the important design choices are fixed ; there may be many sets of reasonable design specifications which cannot be specified by the available parameter choices; the designer may only be permitted to make crude tradeoffs among performance specifications.

A practical analog synthesis tool must deal with all these concerns ; i.e. unlike digital tools, it must handle performance parameters that constrain continuous quantities(i.e. voltages or currents) and it must adapt rapidly(and automatically) to changes in the fabrication process. In order to achieve these goals, it is necessary to take an entirely different approach to generating a sized transistor schematic from performance specifications for analog circuit modules. This is essentially the top down, knowledge based approach which typically strives to transform specifications to circuit schematics first and then attack layout. Analog circuits have actually provided a useful domain for testing many ideas about constraint propagation [2], causal models and qualitative reasoning. Some attempts, in the past, focussed more on rule based systems e.g. Bowman[3] describes a rule based system that assembles opamps from specialized components pieces, but it is not clear if this methodology can be used in other circuit synthesis tasks. The BLADES system[4] proposes a framework in which individual subcircuit experts are coupled by a design manager to build higher level circuits. BLADES does use some hierarchy, in the form of subcircuit experts, but does not suggest any mechanism by which such experts can

be coordinated to actually perform high level synthesis.

Approaches to analog design using hierarchy as a strong organising principle began to appear around the end of the last decade. Among the first was IDAC[5] which provides a design style for several kinds of blocks e.g. opamps, voltage and current references etc. and can synthesize these circuits to meet user specifications. It uses some limited hierarchy and adopts a two phase synthesis process. First an algorithmic design strategy is executed to size the devices in the fixed schematic ; this is a coarse design. If this design is deemed close enough to specifications, a second numerical optimization phase is performed to tune the final circuit. OASYS[6] does some limited numerical optimization and since it uses less of flat circuit details for tuning to correct failures. A lot of progressive iteration is done at each level of the design in each subblock of the design in OASYS. This adds to the CPU time in designing the circuit and makes the overall design costlier.

The approach adopted in the present work is to retain the hierarchical design notion suggested in OASYS in that each sub-block of the design is capable of being designed separately and being reused as a part of a higher level circuit but some design tricks that can be used over various levels of hierarchy especially for the design of such blocks which are tightly bound to a particular topology are used. The use of such design knowledge obviates the need for repeated iterations as the design obtained is quite close to specifications after the first phase. This strategy thus reduces the cost of the design.

Among the other related tools, OPASYN[7] models the overall synthesis tasks as a large set of tightly coupled nonlinear equations and relies primarily on numerical techniques for solution. Our approach is similar to OPASYN in that a simple rule based style selection mechanism is adopted, but OPASYN adopts no hierarchy and no direct reusability of previously coded design knowledge. AN-COM [8], which appeared after OPASYN, somewhat resembles OASYS, in that it has a general

hierarchy search mechanisms to refine down this hierarchy and failure handling mechanisms. However it is unclear if AN-COM is capable of negotiating trade-offs iteratively, up and down the hierarchy to optimize performance.

More recently, some new approaches for automated circuit sizing have been suggested, using a symbolic simulator, which automatically generates all characteristics in the analytical model of the circuit, in an optimization program[9]. Optimization time is strongly reduced by replacing the full numerical simulation at each iteration with an evaluation of the analytical model equations. However, the exponential growth of the number of terms with the circuit size in expanded symbolic expressions makes the evaluation of such expressions for automatic circuit sizing less efficient than a simple numerical simulation. Sensitivity rating algorithms, through the identification and extraction of those designable parameters which most affect circuit performance, used in OPASYN[7], have more recently been used for automated transistor sizing[10]. However, it is unclear whether a large population of aggressive designs could be completed using this approach.

Chapter 3

KANSYS ANALOG SYNTHESIS FRAMEWORK

The specific goal of KANSYS is to convert a behavioural circuit description into a specific structural description ; i.e. the inputs to the KANSYS synthesis framework are circuit performance specifications and the output is a sized transistor level schematic.

Since KANSYS is based upon analytical approximations that characterize the behaviour of specific circuit topologies, the circuits designed by KANSYS may not meet all of the performance specifications. This is not a significant drawback to this approach for several reasons. First the designs produced by KANSYS can be further refined by using conventional circuit optimization tools[11]. The prime goal is to choose the best topology and to choose device sizes that are approximately correct. Secondly due to the wide variations in process parameters there are always variations in the performance of analog circuits.

The important requirements for a general framework for analog circuit design are

1. It must provide a uniform structured view of synthesis.

2. It must compartmentalize design knowledge, which facilitates the addition of

new knowledge and modification of existing knowledge.

3. Design knowledge must be reusable : it should be acquired once and available everywhere.

4. It must be easy to extend design knowledge : easy to add new knowledge and easy to modify existing knowledge.

The key ideas that underlie the KANSYS framework are :

1. Analog circuits do admit a hierarchical decomposition.

2. For any circuit design there exists a group of known block level topologies, one of which may be selected.

3. Equation based methods can be used to translate specifications from one level in the hierarchy to the lower level.

3.1 Hierarchy

Unlike digital circuits, analog circuits do not generally have a universally agreed upon and unique hierarchical decomposition : e.g. some researchers view an opamp as made up of stage-1 and stage-2 while others decompose the opamps into differential pairs, current mirrors etc. However hierarchical decomposition does play a very important role in the way human analog circuit designers attack the design task.

Reliance on explicit hierarchy in analog circuit design has two advantages. First it permits the design process to be recast as a sequence of smaller design tasks alternating between design style selection and translation. Second, it provides a measure of generality, in that the subblocks can be reused in different contexts. In the analog domain, there is no single, accepted hierarchical structure agreed upon by

the community at large ; rather the best hierarchical decomposition for a particular analog circuit is part of the domain knowledge for the design of that circuit, i.e. it is derived from the expertise of the designer.

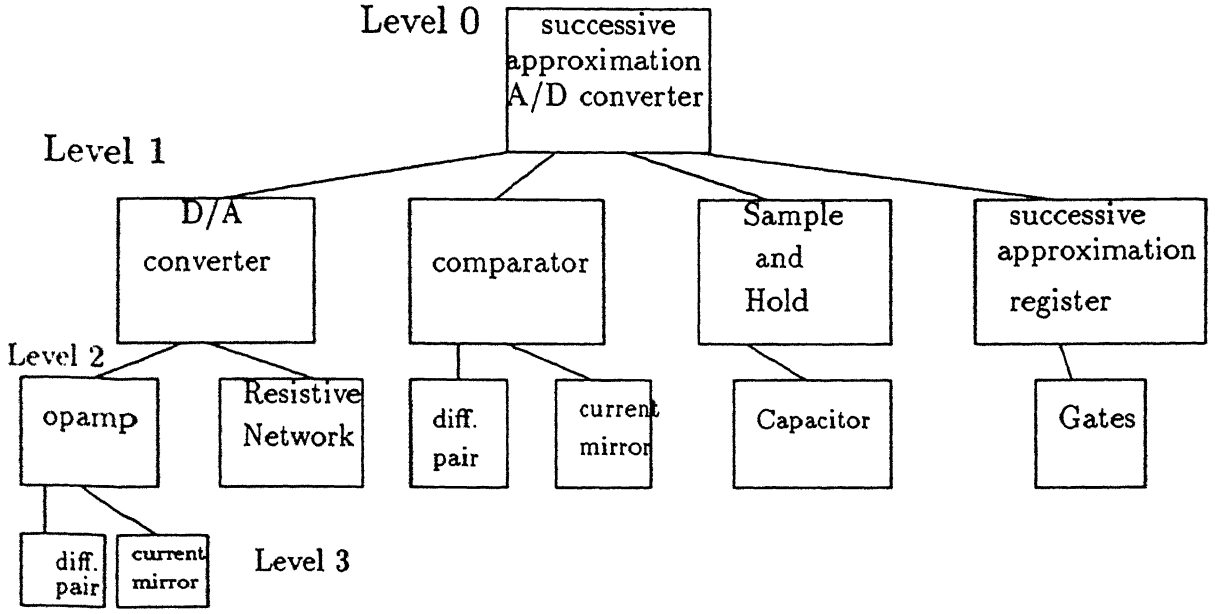


Figure 3.1: Example of hierarchy in analog circuits

A hierarchical representation makes the synthesis task more tractable, but it has disadvantages also. Optimizing the choice of sub-block performance is more difficult in a hierarchical structure than in a flat transistor level schematic e.g. the intermediate level shifter block in an opamp which depends on the dc biases to be present at the input and output is tightly bound to a particular parent style. A second potential drawback of a hierarchical structure is that it does not employ design tricks in which knowledge about choices made in one sub module influence choices made in another sub module. Expert circuit designers employ design tricks that jump across many levels of hierarchy to push circuits close to the limits of achievable performance. In this work, we have tried to compensate for this disadvantage by retaining a part of the design knowledge across many levels of hierarchy. However

this, in no way prevents the sub-blocks from being reused as a part of higher level design. The second problem is taken care of by a careful choice of hierarchy.

3.2 Design style selection

A design style is an interconnection of abstract blocks. Because of the hierarchical decomposition, design styles are topologies of connected blocks, not transistors ; i.e. choosing a design style is not choosing a transistor schematic. The KANSYS system relies on the existence of mature design styles at each level of hierarchy for the analog circuit modules to be designed.

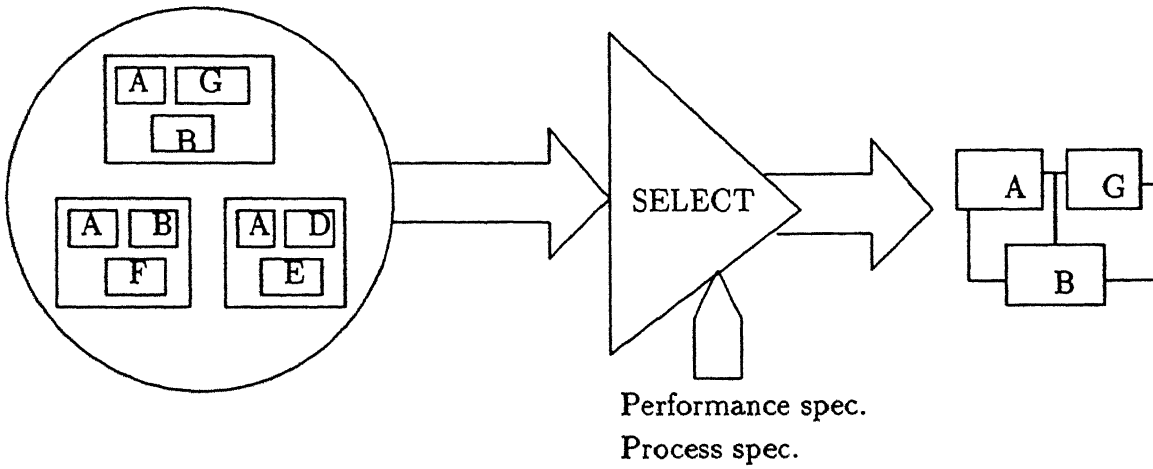


Figure 3.2: Example of design style selection

Typically at any level in the hierarchy, there are several design styles available to implement a particular function e.g. we have two design styles for a current mirror, standard current mirror and a cascoded current mirror. These different styles provide the same functional behaviour but offer different performance tradeoffs.

At any point in the design process, we must design a block with some desired functional behaviour. In KANSYS, we first select one of the available design styles to pursue based on the necessary performance specifications. In addition since the

selected design styles might fail to meet our performance specifications, we must detect design styles that are incompatible with the specifications and — to the extent possible — rank the compatible ones . For example, if the design specifications for an opamp requires differential outputs, then an opamp design style with only a single ended output is incompatible.

3.3 Translation

Having selected an interconnection of sub-blocks , the next step in the design process is the determination of performance specifications for each of the sub-blocks that make up the selected design style. We define this process as translation of the performance specifications at the block level into a set of performance specifications at the sub–block level. The translation process must guarantee that if sub-blocks

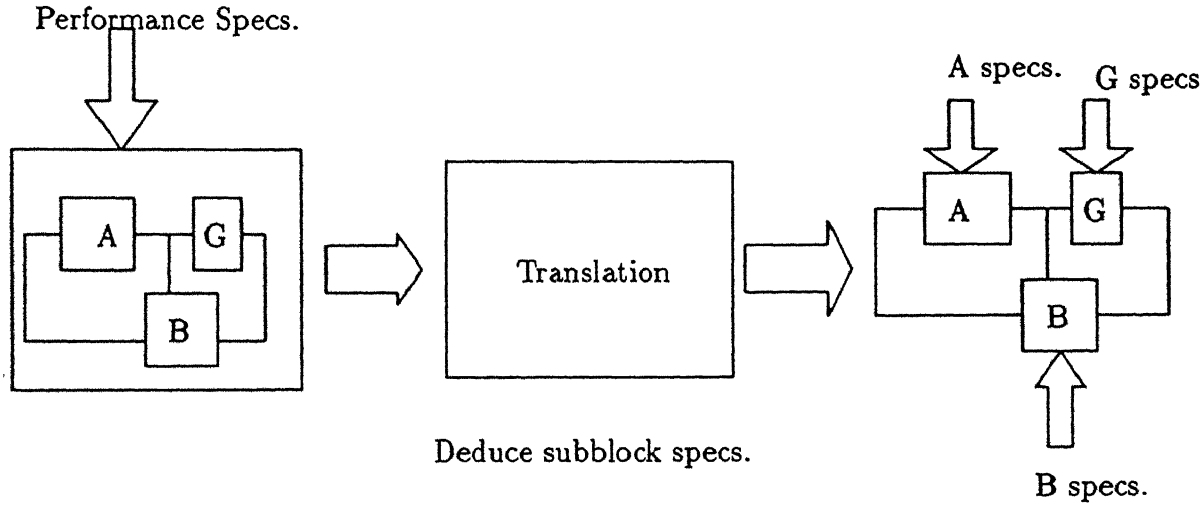


Figure 3.3: Example of translation of specifications

with the chosen performance specifications are connected in the manner indicated in the design style, then the block will meet its performance specifications.(Fig 3.3)

As an example of the process we consider the simple two stage opamp. This

opamp consists of fixed configurations of building blocks such as current mirrors, differential pairs, bias networks, loads, gain stage. The transistor sizing is done in two steps : first opamp performance specifications will be used to design the sub-blocks : second the specifications for each sub-block can be used to design the transistors that comprise each of the sub-blocks. It is important to recognize that "to design" in this translation process means "to produce performance specifications for". For example, the input specifications for an opamp are dc gain, slew rate, unity gain frequency, phase margin etc. For a two stage opamp design style selected, the translation process for the differential amplifier block involves the specifications of the gain required of the differential amplifier(the other part of the gain being provided by the output buffer.), the unity gain frequency, the CMRR and the input transconductance of the differential pair. We should carefully note that for this choice of hierarchy, the input specifications for the differential amplifier, designed independently, would not include the input transconductance of the differential pair. This is a feature introduced to eliminate the problem in hierarchical design as discussed before(see section 3.1).

Similarly the specifications for the gain stage involves the specifications of the gain required and the current value as fixed by the other parts of the circuit. These individual blocks have their own translation tasks to perform; they must translate the input specifications to width(W) and length(L) specifications for the MOS devices. When we reach this point in the sequence of translation steps, we are done, since W & L specifications for each device constitute a finished sized design.

KANSYS translation mechanism are most similar to the hierarchical planning mechanism suggested in Brown's notion of routine design[12]. The important idea behind all these systems is that some design domains are characterised by the existence of mature plans of attack for broad classes of problems. By organising the overall design task as levels of coarse to fine refinement i.e. by organising the prob-

lem hierarchically, we can bring those mature plans to bear on problems too complex to solve in a single refinement step.

There are, however, some important differences in how KANSYS adapts planning ideas to handle hierarchical refinement for analog design. These differences center on the granularity of the individual design steps in each plan. In [12], the grain size appears to be fairly large. In contrast, analog design has an explicitly fine grained character.

3.4 Completing the design

A complete design consists of a hierarchical decomposition, and a set of design style selections and associated translations. We start by selecting a design style for the block, which consists of an interconnection of sub–blocks. We then translate block specifications into sub–block specifications. Thus for each sub–block we select a design style for that sub–block, each of which consists of an interconnection of sub–sub–blocks. We then translate sub–block specifications into sub–sub–block specifications for each sub–sub–block. The process of selection and translation continues till we reach primitive components at the element level ; e.g. transistors, C's, R's. Only at this bottom level does translation correspond to device sizing. Note that since the analog hierarchy is not strict (i.e. uniform in depth along each branch), the component level may be reached at different depths along different branches.

The complete synthesis process is shown in the block diagram:

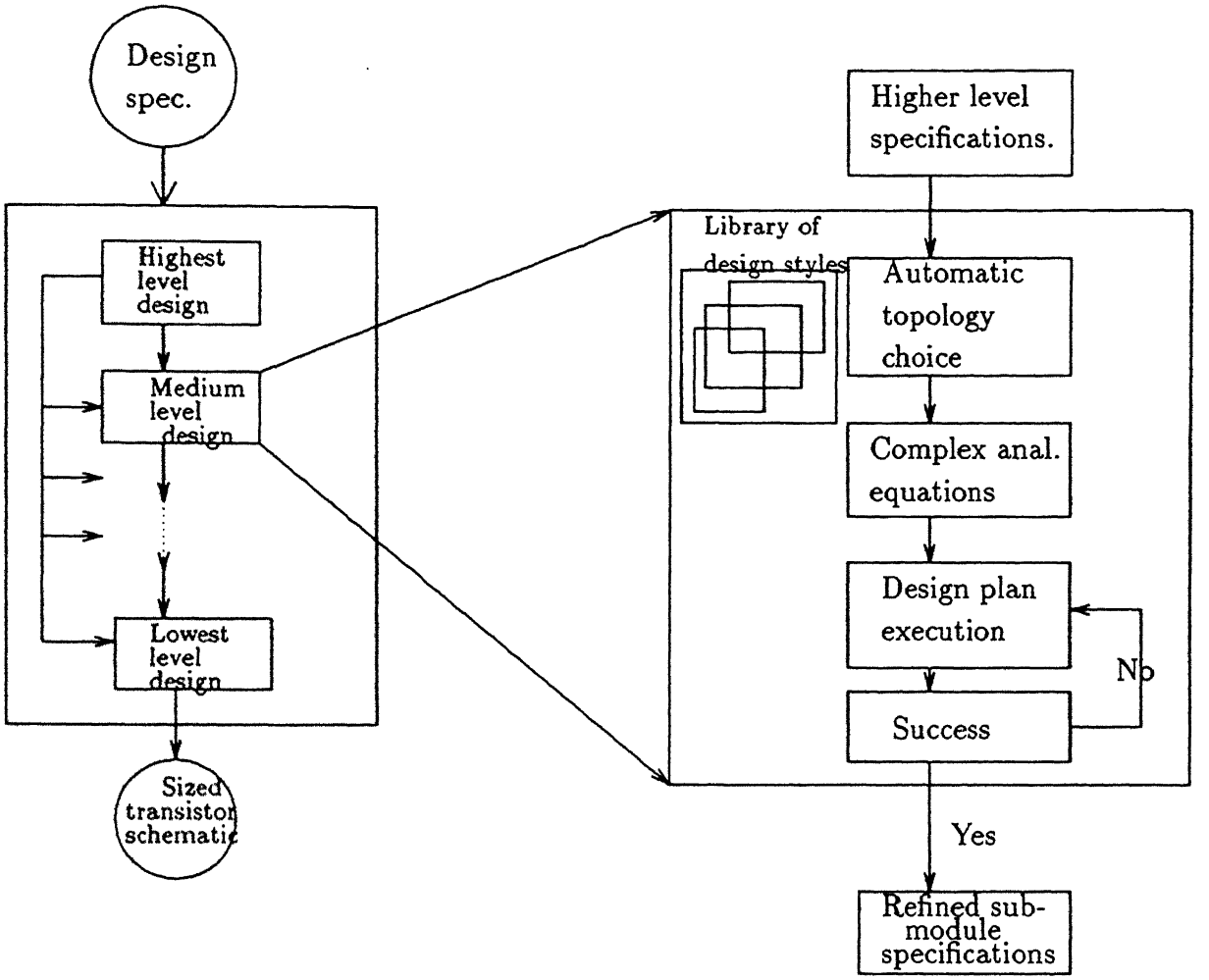


Figure 3.4: Block diagram of KANSYS framework

Chapter 4

A FEW DESIGN EXAMPLES

KANSYS is capable of synthesizing the following circuits from user specifications:

1. Bias circuits
2. Level shifter
3. Gain stage
4. Current mirror
5. Differential Amplifier
6. Operational Amplifier
7. Sample and hold
8. Digital to Analog converter
9. Filters - Low pass, High pass and Band pass

The user is first required to enter the process specifications like the transconductance factor k_p, channel length modulation factor λ and the threshold voltage V_T for both the nmos and pmos devices. The performance specifications are entered after that. However each of the specifications should be entered in a permissible

range which is for most of the cases, general enough to include all the practical behavioural specifications. We discuss the design examples of differential amplifier, operational amplifier, digital to analog converter and the Sample and Hold circuits to illustrate our design strategy. Out of these, two different topologies have been implemented for the differential amplifier and five different topologies for the operational amplifier. Here topology means the connection of sub-blocks which may again be implemented in several different ways. So the actual number of flattened designs is larger in number. The output of KANSYS is in the form of sized transistor design in a SPICE file so that the circuit can be checked by immediate simulation.

4.1 Differential Amplifier design

We first present the simple differential amplifier design and then the more complex differential amplifier with cascode load design.

The differential amplifier accepts three process specifications and six performance specifications if designed independently and seven performance specifications if it is being used as a sub–block in a higher level design. The following are the performance specifications for the differential amplifier :

1. The differential gain, A_d
2. The Common mode rejection ratio, CMRR
3. The unity gain frequency, UGF
4. Current, I_o
5. Capacitor load, C_L
6. Power supply

The seventh performance specification, which is used when the differential amplifier is being reused in a higher level design, is the input transconductance of the differential pair.

The process specifications are the following :

1. The transconductance factor, k_p
2. The threshold voltage, V_T
3. The channel length modulation factor, λ

The following steps are involved in the design of differential amplifier:

1. Calculate the input transconductance factor G_{mi}, if not already specified, using the equation $A_d = g_{mi}/2\lambda I$. If this is not consistent with the specifications of UGF and C_L according to the equation $g_{mi} = \omega_o C_c$, we adjust the value of the current required.
2. Using the above value of the transconductance determined, the aspect ratios of the input differential pair can be determined using the following relation

$$G_{mi} = 2\sqrt{k(1 + \lambda V_{DS}^{\circ})I_D^{\circ}} \simeq 2\sqrt{kI_D^{\circ}}.$$

   taking into account only the first order effects. Here $k = k_p(W/L)$. Keeping the minimum feature size specification as the value for L, the width of the devices can be ascertained.
3. The load transistors are the current mirror devices which should be matched to produce the desired characteristics. For this case the output resistance of the mirror is just the incremental drain resistance of the PMOS device which depends on the channel length modulation and the current. Since we should have both the PMOS devices also in saturation, we arbitrarily allow

a drop of $|V_{GS} - V_T| \sim 0.5$ (for 5v supply). Knowing the drop and the current through the devices, the sizes can be determined using the equation $I_D = k_p(W/L)(V_{GS} - V_T)^2$.

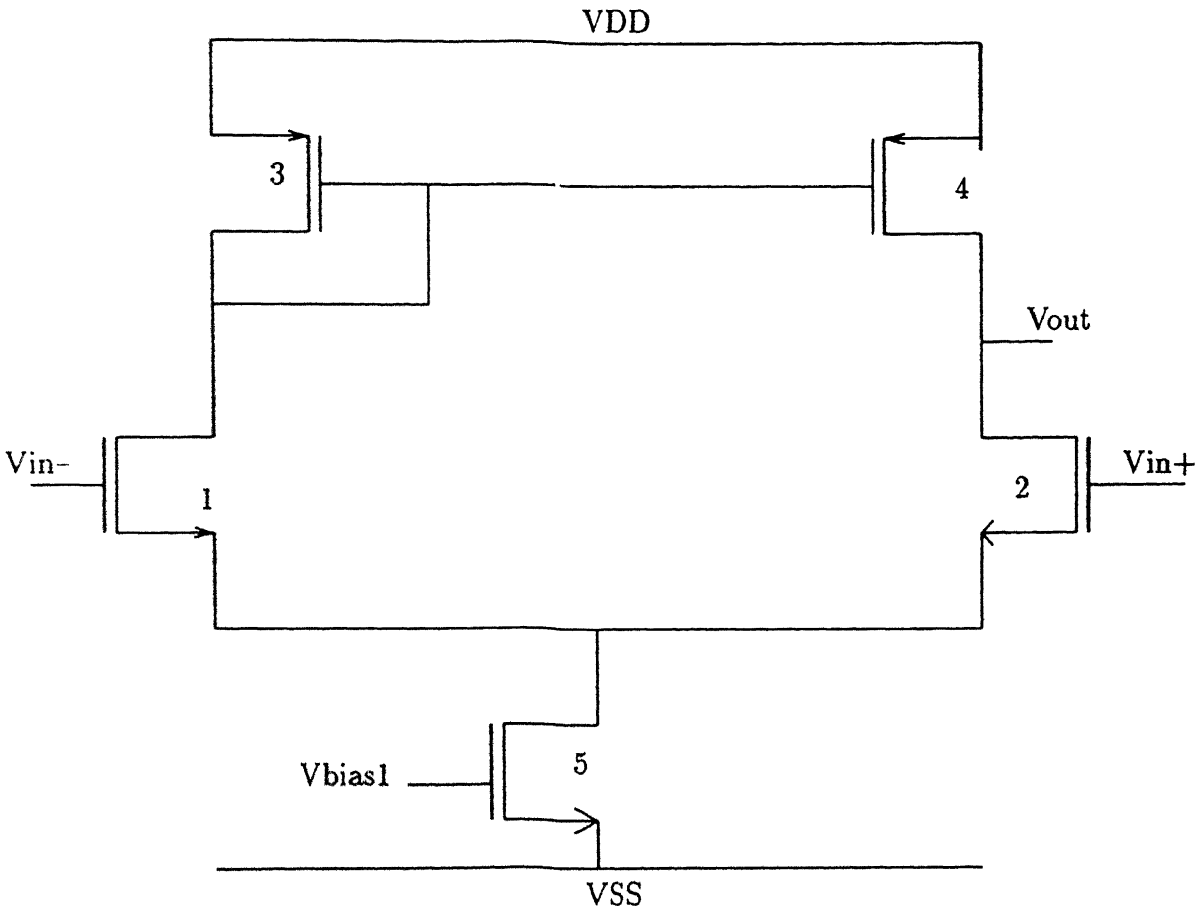


Figure 4.1: Simple differential amplifier topology

4. Similarly the drop across the current source nmos device can be determined by assuming the same $|V_{GS} - V_T|$ drop. Knowing the drop across the current source we can determine the required bias voltage and design the appropriate bias circuit by specifying the bias voltage and current.

We use the following expression for the CMRR to check whether the design is

consistent with the specifications.

$$CMRR = 2(g_{mi}g_{m3}/g_{d5}g_{di}).$$

Knowing the sizes of the devices we can calculate all the above parameters and hence the CMRR. If this satisfies the specification, then the design is good, otherwise the drop $|V_{GS} - V_T|$ can be adjusted for the current mirror and current source transistor to achieve the desired CMRR.

Note that step 5 constitutes a simple form of fixed iteration; it always works in the range specified by KANSYS, as has been checked by extensive simulation.

If however, the input specifications are such that the differential amplifier with cascode load is selected, then the following design strategy is adopted.

The following steps are taken in the design of this differential amplifier.

1. The input transconductance g_{mi}(if not specified by a higher block) can be determined by the equation $g_{mi} = \omega_o C_L$.

2. The aspect ratios and hence the sizes of the input transistors can be determined using the relation

$$g_{mi} = 2\sqrt{kI_d^o}.$$

as before.

3. The size of the current source transistor can be determined as before by assuming the drop $|V_{GS} - V_T| \sim 0.5$ (for 5v supply). Knowing the drop across the current source, we can determine the required bias voltage V_{Bias1}. The bias voltage V_{Bias2} can also be fixed at some value in the same way and specifying the appropriate bias voltage and the current for the bias circuit, the bias circuit can be determined.

4. The composite load forms the cascode current mirror which is responsible for the high output resistance of the differential amplifier. The output resistance is determined by the following expression:

$$R_o = 1/(g_{d4}/g_{m6}r_{d6} + g_{d2}/g_{m8}r_{d8}).$$

Using the expression and the following assumptions:

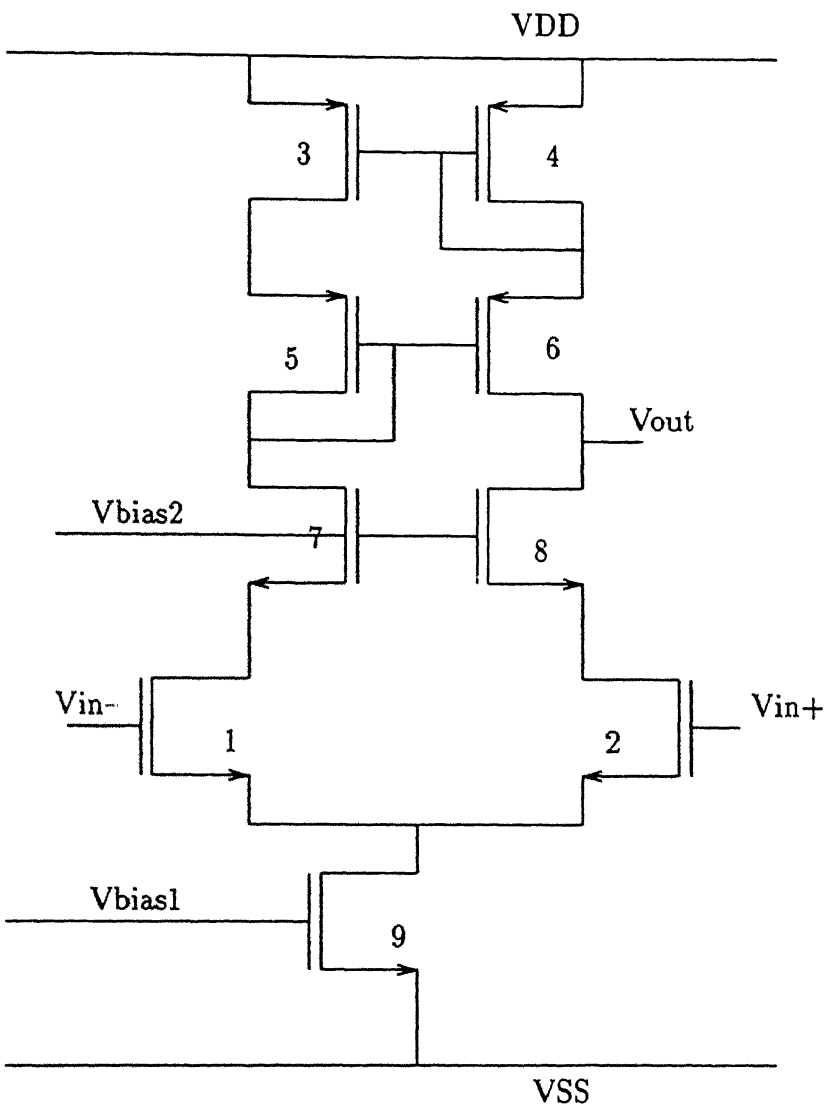


Figure 4.2: Cascode differential amplifier topology

$$(W/L)_1 = (W/L)_2$$

$(W/L)_3 = (W/L)_4$

$(W/L)_5 = (W/L)_6$

$(W/L)_7 = (W/L)_8$ (matched transistor requirements)

and also that $|v_{gs} - v_T|$ drop for the transistor M_7 and M_8 is almost the same as M_9 and thereby

$$(W/L)_7 = (W/L)_9/2$$

the sizes of the transistors can be determined.

It has been checked by detailed simulation that this strategy of design works well for all the values in the range specified. However the range of specifications allowed in this case is limited owing to two reasons : firstly a lot of assumptions have been followed in the design which may not be true for the values outside the range and secondly we have been unable to interface SPICE simulation inside the software owing to the absence of the command file which should be provided with the software.

4.2 Operational Amplifier design

Opamps were first chosen as the initial target for the KANSYS because they are ubiquitous components in many system level designs and because they appear to be the first target of earlier synthesis approaches[3],[6],[7],[13]. KANSYS currently incorporates five basic topologies for the opamps.

1. Simple two stage.

2. Two stage with level shifter.

3. High gain opamp with cascode load in the differential amplifier.

4. Wideband folded cascode opamp.

5. Differential output opamp.

Of these topologies, the high performance opamps, especially the high gain opamp, have been automated for limited ranges for reasons mentioned before (section 4.1). Even for these limited choices of design styles, the hierarchical decomposition of styles leads to several different transistor level opamp topologies, except for wideband folded cascode opamp and the differential output opamp which have been implemented on fixed topology scheme.

We discuss here the design strategies of the 2^{nd} and 3^{rd} schemes only. SPICE output files produced by KANSYS for different sets of performance specifications are presented, however, for all the schemes.

The input specifications for the operational amplifier include, apart from the three process parameters, the following:

1. The dc gain, A_d
2. The unity gain frequency, UGF
3. The slew rate, SR
4. The phase margin, ϕ
5. The capacitive load, C_L
6. Common mode rejection ratio, CMRR
7. Power supply
8. Differential output requirement.

Before going on to the selection of design styles for the opamps, we first translate the behavioural specifications to some of the circuit parameters using the following equations.

1. Current of the current source $I_o = (SR) * cap.$

2. Input transconductance of the differential pair $g_{mi} = \omega_o C_c$

Now depending on the behvioural specifications and the above parameters, one of the five basic topologies is chosen. If scheme 2 is selected the following steps are executed:

1. The first step would require the translation process for the differential amplifier design. The differential gain required of the differential amplifier A_{d1} can be calculated by using the equation

$$A_{d1} = g_{mi}/(2\lambda * I_o/2) = g_{mi}/(\lambda * I_o)$$

The other parameters required are the CMRR, which is reduced by the same amount as A_{d1} is from A_d, the unity gain frequency and the capacitor, which are kept the same, and the current value, which is as calculated before design style selection of the opamp. Thus a sub-block of the opamp is ready.

2. For the design of the gain stage, the gain required A_{d2} is calculated as follows $A_{d2}(db) = A_d - A_{d1}(db)$. However since the design of the gain stage is tightly coupled to the opamp specifications, the required value of current, I_{Bias}, is obtained in two iterations.

   (a) The output transconductance is given by

$$g_{mout} = ([tan^{-1}\phi] + 1)\omega_o C_L;$$

   (b) The value of I_{Bias} is calculated from the equation :

$$g_{mout} = 2I_{Bias}|V_{GS} - V_T|.$$

For the device to be in saturation, we allow the drop $|V_{GS} - V_T|$ to be 0.5 (for 5v supply)

(c) However to provide the gain A_{d2}, the transconductance should be greater than $comp = 2\lambda I_{Bias} A_{d2}$.

(d) We choose, therefore, the maximum of g_{mout} and comp and assign the value to g_{mout}. If comp is much greater than g_{mout} the degradation in phase margin would be large.

(e) I_{Bias} is now calculated from this value of g_{mout}.

The translation parameters for the design of the gain stage are now available and the gain stage block is now ready.

3. For the design of the level shifter, the required parameters are the input dc bias level and the output dc bias level. We allow a drop of $|V_{GS} - V_T|$ equal to 0.5 for both the current mirror load transistor and the gain stage nmos device. The drain of the current mirror load Q_4 is held at the same voltage as the gate as Q_3 and Q_4 (see Fig. 4.4) are matched. Thus both the input and output voltages are known. The current through the two devices is assumed to be the same as calculated before design style selection. Thus the sizing of the devices used in the level shifter can be done.

4. Design of the compensation network :–

   (a) The compensation network is modelled as a resistor capacitor combination, with the resistor being implemented by the channel resistance of a pmos device. For the zero, introduced by the compensation network, to cancel the pole s_{p_2} introduced by the output pmos device, the following expression must hold:

$$R_c = 1/|s_{p_2}|C_c + 1/g_{m6} \simeq 2/g_{m6}.$$

   Since the transconductance of the output pmos device is known, we can determine the value of R_c.

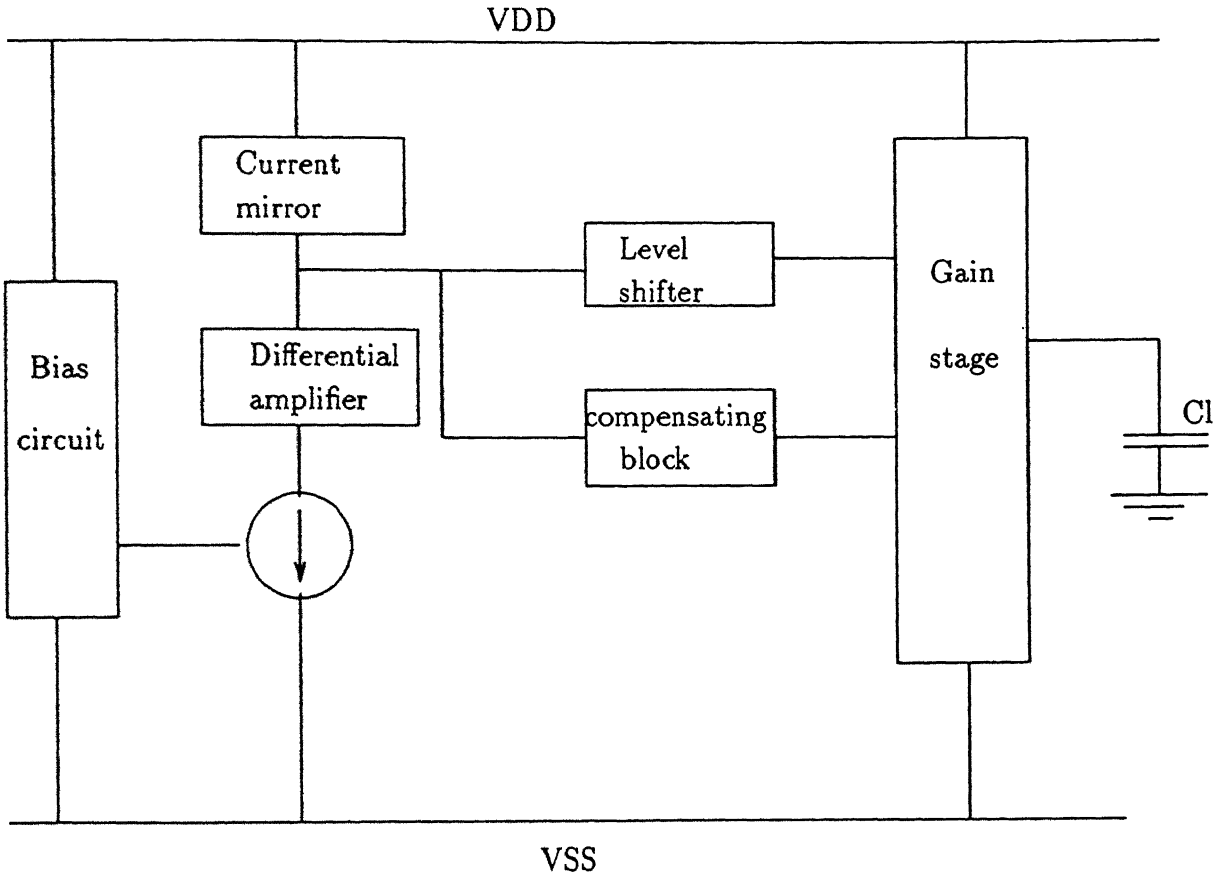


Figure 4.3: Block diagram of two stage opamp with level shifter

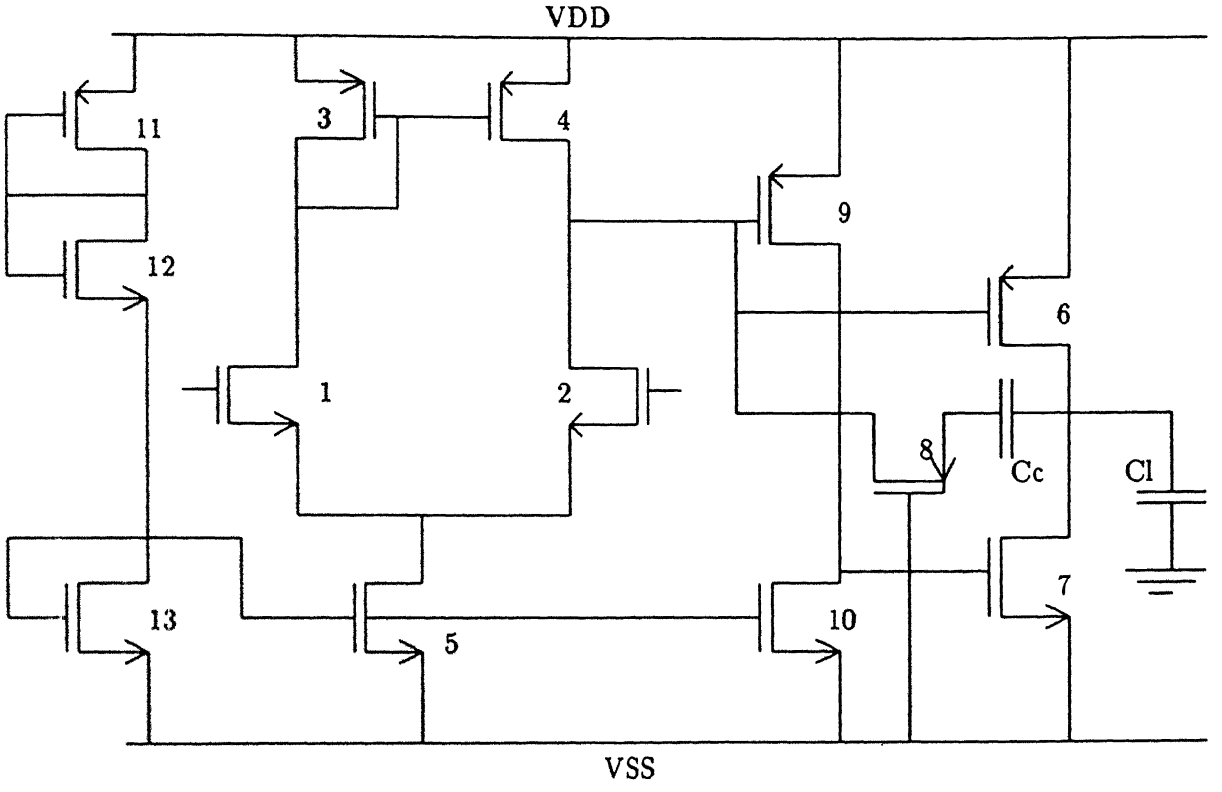


Figure 4.4: One of the implementations of the block diagram

(b) Since the value of R_c is related to the device size by the relation

$$1/R_c = 2k_p(W/L)(|V_{ss} - V_{ds}| - |V_T|)$$

and since V_{ds} is at the same voltage as the drain of current mirror device, which has already been determined, the aspect ratio of the device and hence the sizes can be determined. The compensating capacitor value is taken as approximately the same as the load capacitor.

5. Knowing the value of the bias voltage required, the required bias circuit can be designed. The current through the bias circuit is kept the same as that through the input pair of the differential amplifier.

The opamp design is now complete. The block diagram of this particular design style and one of the possible designs are shown in figures 4.3 and 4.4

If however scheme 3 is selected, the range of specifications for which the design has been automated is limited. The following steps are used in the translation and design plan execution.

1. Translation of specifications to the differential amplifier :-

   (a) From the already determined parameter g_{mi}, we can have a rough estimate of the gain required of the differential amplifier stage using the design knowledge that the output resistance is of the order of 100MΩ($A_{d1} = g_{mi}R_o$)

   (b) Among the other parameters, CMRR is reduced by the same factor as A_{d1} is reduced from A_d, UGF and capacitor specifications remain the same and the current and g_{mi} parameters are as determined before the design style selection of the opamp.

The translation process for the differential amplifier over, it should be noted that since the specifications for the gain required of the differential amplifier

was based on a rough estimate of $R_{out} \simeq 100M\Omega$, it is necessary for it to be within the limits of achievable performance. The differential amplifier with cascode load generally provides gain between 70db and 100db and therefore the input gain specification for the differential amplifier is limited in this range, i.e. if by the equation $A_{dl} = g_{mi}R_o$, the gain goes out of range, it is restricted to end values.

2. For the translation of parameters to the gain stage block, we follow the same procedure as detailed in the design of scheme 2.

3. The required parameters for the design of level shifter block are the input and the output dc level. The input dc level is very hard to determine and we, therefore, use the simplifying assumption that the drops across both the pmos devices which form the composite loads in the differential amplifier are equal. The output dc level of the level shifter is however calculated by using the design of the output gain stage and the equation

$$I_{out} = k_p(W/L)_p(V_{GS} - V_T)^2.$$

Knowing $(W/L)_p$, the drop $V_{gs} - V_T$ and hence the output dc voltage of the level shifter can be determined. The current through the two devices is the same as calculated before design style selection. Thus the sizing of the devices in the level shifter can be done.

4. The compensation network can be designed in the same manner as detailed in the design of two stage opamp with level shifter.

5. The bias circuits are designed as a part of the differential block. Also a bias circuit is needed for the level shifter block which would be different from the bias circuit designed for the differential amplifier design. This bias circuit is designed as a part of the level shifter block.

One of the possible topologies for the opamp scheme 3 is as shown:

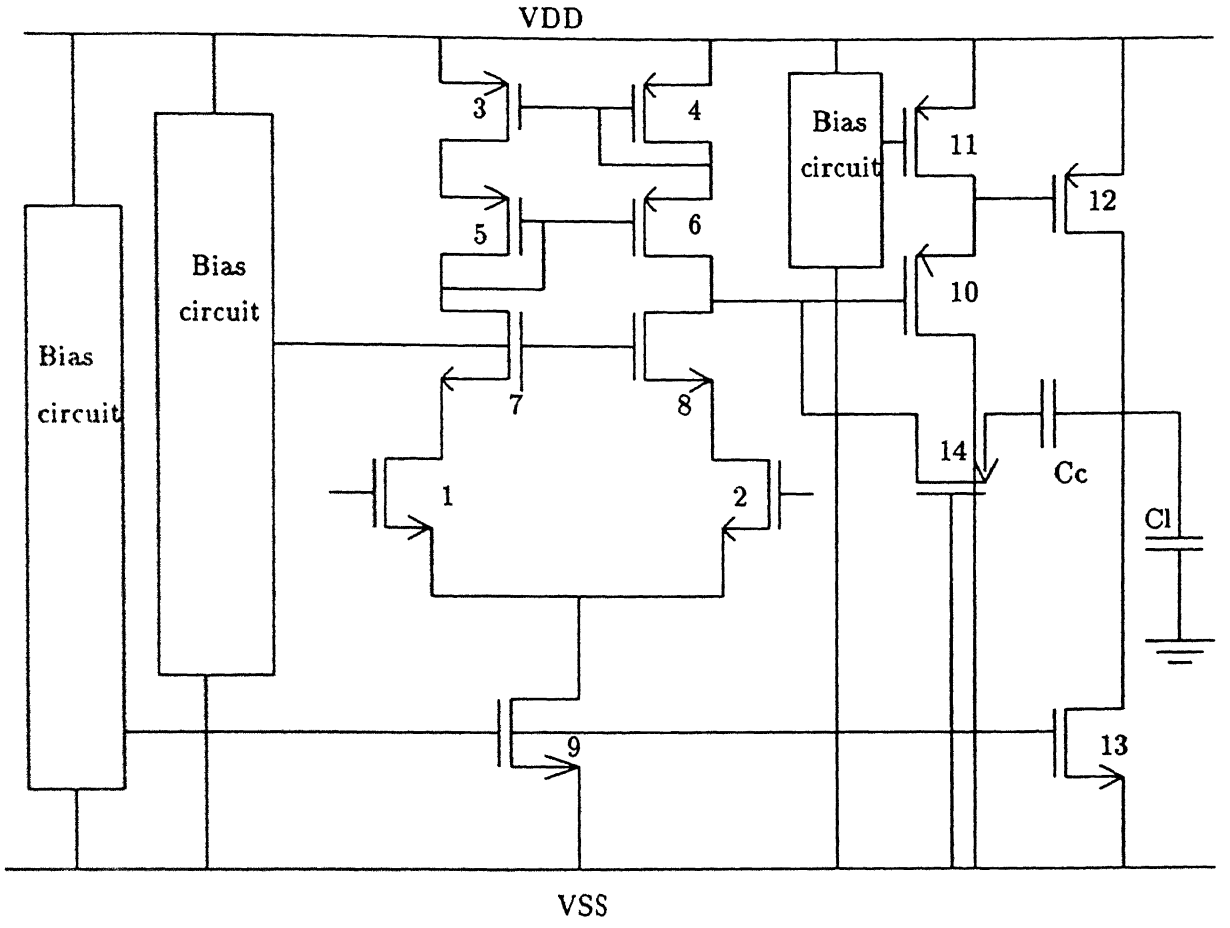


Figure 4.5: One implementation of opamp scheme 3

The other schemes for the opamps like the wideband folded cascode opamp and especially the differential output opamp use limited hierarchy and more of flat circuit optimization techniques. This is not because of any shortcoming in our framework but because of the absence of well defined hierarchy as compared to the two stage or high gain opamp. Also some parts of the circuit, such as the bias chain in the fully differential opamp[18], are inseparably coupled with the flattened circuit. We do not discuss the designs of these schemes over here. However sized transistor schematic

synthesized by KANSYS are presented for a particular set of specifications for each of these schemes in chapter 5.

4.3 Design of macrocells

The macrocells designed are sample and hold, digital to analog converter and active filters. We discuss here the design of digital to analog converter and sample and hold circuit only.

Digital to analog converter:

The digital to analog converter consists of an opamp, a resistor ladder network and mos switches. The input specifications are the input bits. We consider the design of a 10 bit D to A converter. The following are the key steps in the design.

1. Here the translation of parameters to the opamp block is motivated by qualitative considerations, i.e. the amplifier should have low input offset voltage as also the following features[17]

   (a) Sufficiently high open loop gain (~80db)

   (b) High slew rate and low settling time.

   (c) Single ended output.

   The design style selected is two stage opamp with level shifter primarily because high slew rate is achievable and because of the low input offset voltage associated with it (<0.5mv). High gain opamp(scheme 3) would have been better choice for the low input offset voltage but then high slew rate has not been automated for this amplifier.

2. Design of the switches :-

(a) The switch used for the D/A converter is single pole, double throw switch. (see Fig. 4.6) When the digital input is high, M_1 is ON and the arm of the ladder S is connected to GND whereas when the input is low, pmos transistor M_2 is ON and the ladder arm is connected to V_{REF}.

The resistance of a transistor in linear region is given by
$1/R_d = k_p(W/L)(V_{GS} - V_T)$ for nmos device, and
$1/R_d = k_p(W/L)|V_{GS} - V_T|$ for pmos device.
For $V_{REF} = V_{SG} = 4v, R_d = 9661.84/(W/L)_p$ for $k_p = 60\mu A/v^2$ and $V_T = 1.2v$.

Because of sensitivity to temperature and larger tolerance associated with larger value of channel resistance, which might well degrade the overall accuracy of D/A converter, a small value of channel resistance is required. However a small value will require large transistor size and hence larger chip area. Thus making a compromise between (W/L) and R_d, R_d is chosen to be around 500Ω.

(b) The aspect ratio of the nmos device is determined as

$$(W/L) = 1/(R_d * k_p * (V_{gs} - V_T)).$$

Since one end is at ground, $V_{GS} = V_{supply}$.

(c) The aspect ratio of the pmos device is determined by the same equation, except that $v_{sg} = V_{REF}$.

3. The resistive network is a R-2R ladder. We choose R=10k to maintain sufficiently high input resistance of the opamp. Thus the arm resistance value R' =2R-500=19500Ω.

The design for the D/A converter is now complete. The circuit of D/A converter is shown in figure 4.6.

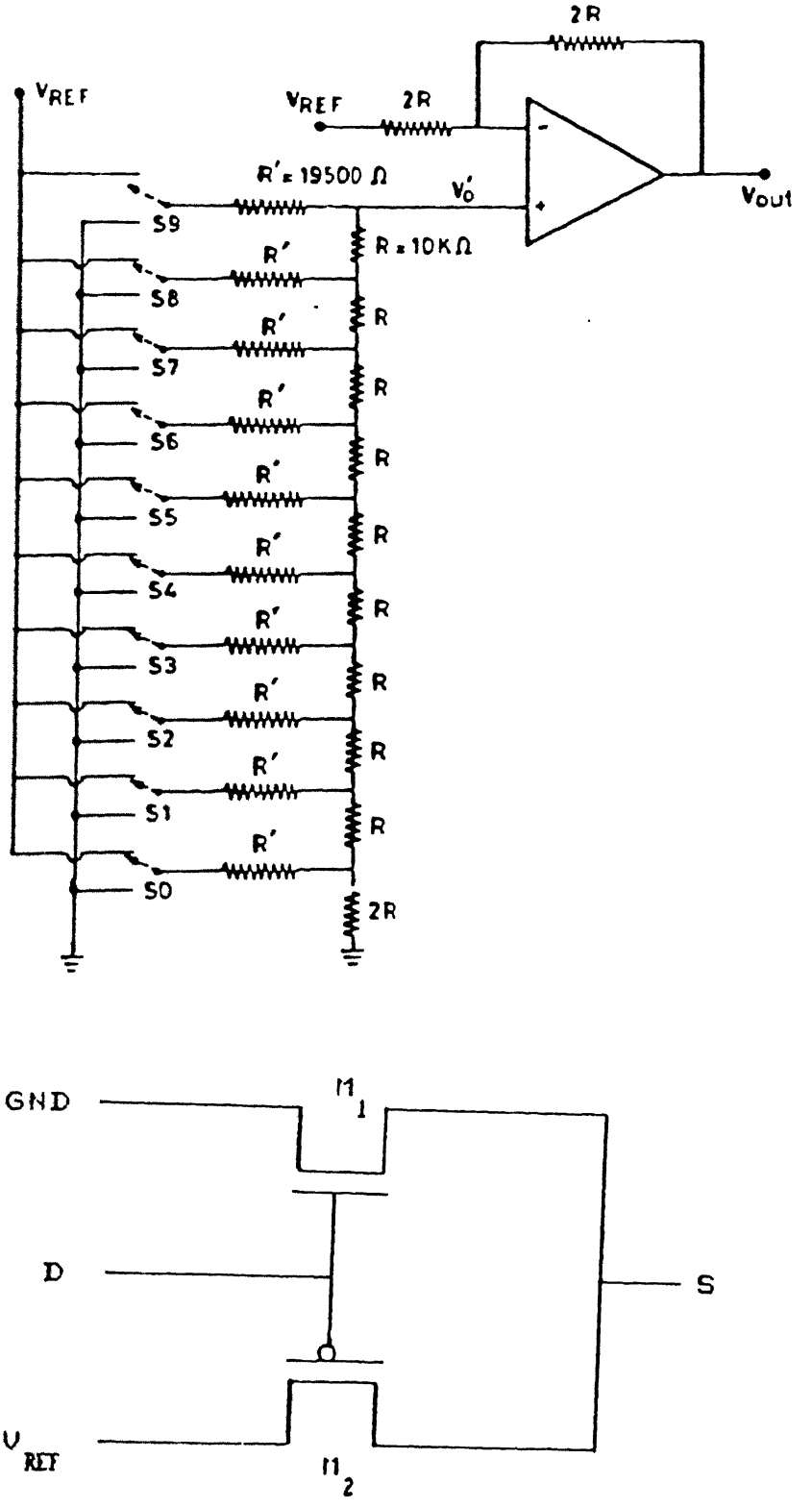


Figure 4.6: Digital to analog converter

Sample and Hold circuit

The amplifier used in the Sample and Hold circuit should have the following features:

1. Low input offset voltage.
2. The amplifier should be designed for large phase margin.
3. The amplifier should be designed for a closed loop gain of 10^4 i.e. around 80db.

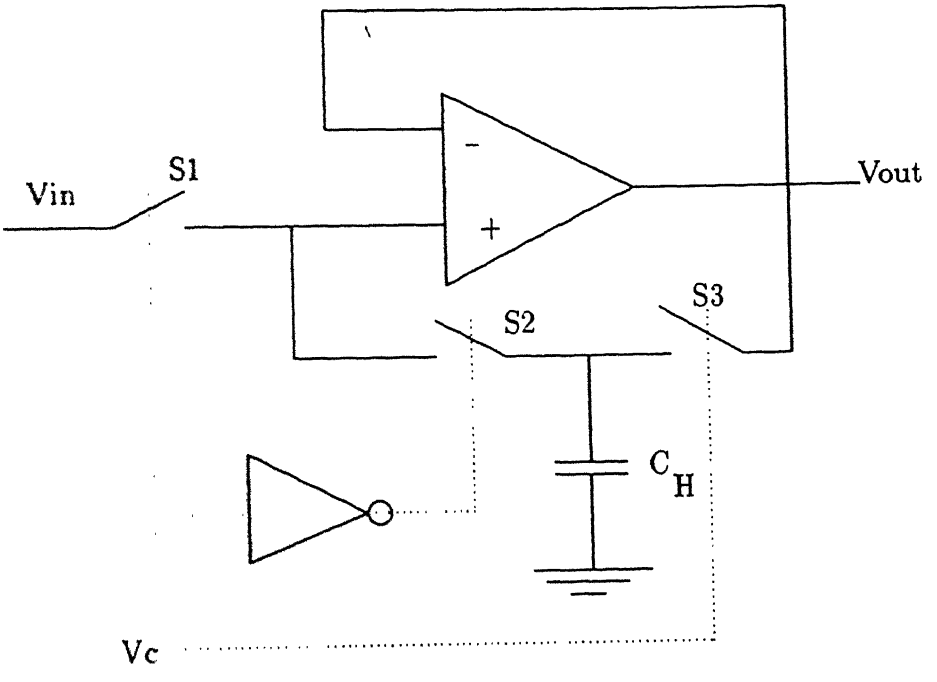


Figure 4.7: Block diagram of Sample and Hold circuit

The following steps are taken in the design of the sample and hold circuit :

1. Translation of specifications to the opamp:- Since a gain of around 80db will do the job, high gain opamp(scheme 3) is not selected. But since the UGF required may vary over a large range, two possible design styles, schemes 2 and 4, may be selected according to the capacitor and UGF value.

2. Design of the switches:-

(a) The design of the switch S_3 is the main consideration as it introduces a pole at $s_p = -1/RC_H$ where R is the resistance of the switch and C_H the hold capacitor. Keeping the pole at slightly above the UGF of the opamp we have the following expression for R.

$$R = 1/(2\pi(1.2f_p)C_H).$$

Also the resistance of the mos transistor in linear region is given by

$$1/R = k_p(W/L)(V_{GS} - V_T)$$

and hence the sizing of both nmos and pmos devices can be done.

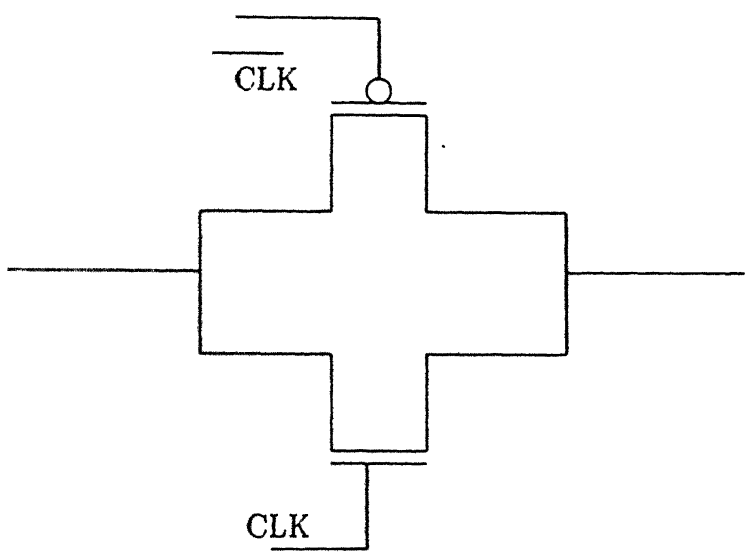


Figure 4.8: Implementation of the switch

(b) Since switches S_1 & S_2 are not required to handle large currents, the (W/L) ratio of these transistors is kept at a minimum to improve the droop rate

Hence $(W/L)_1 = (W/L)_2 = (W/L)_3 = (W/L)_4 = 1$

The design for the sample and hold circuit is now ready. Two possible implementations at the transistor level are shown in Figs. 4.9 and 4.10.

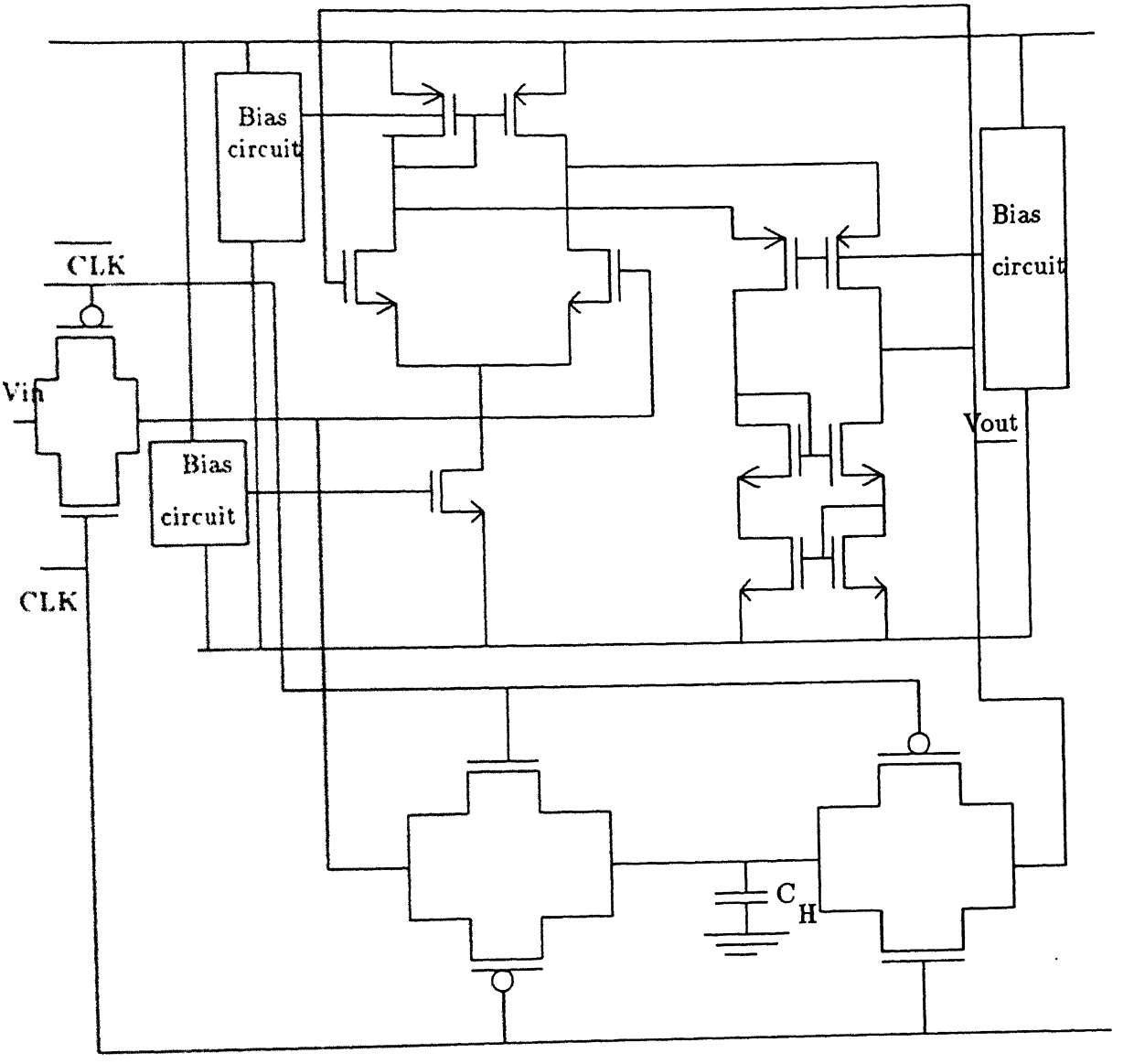


Figure 4.9: S & H circuit with wideband folded cascode opamp

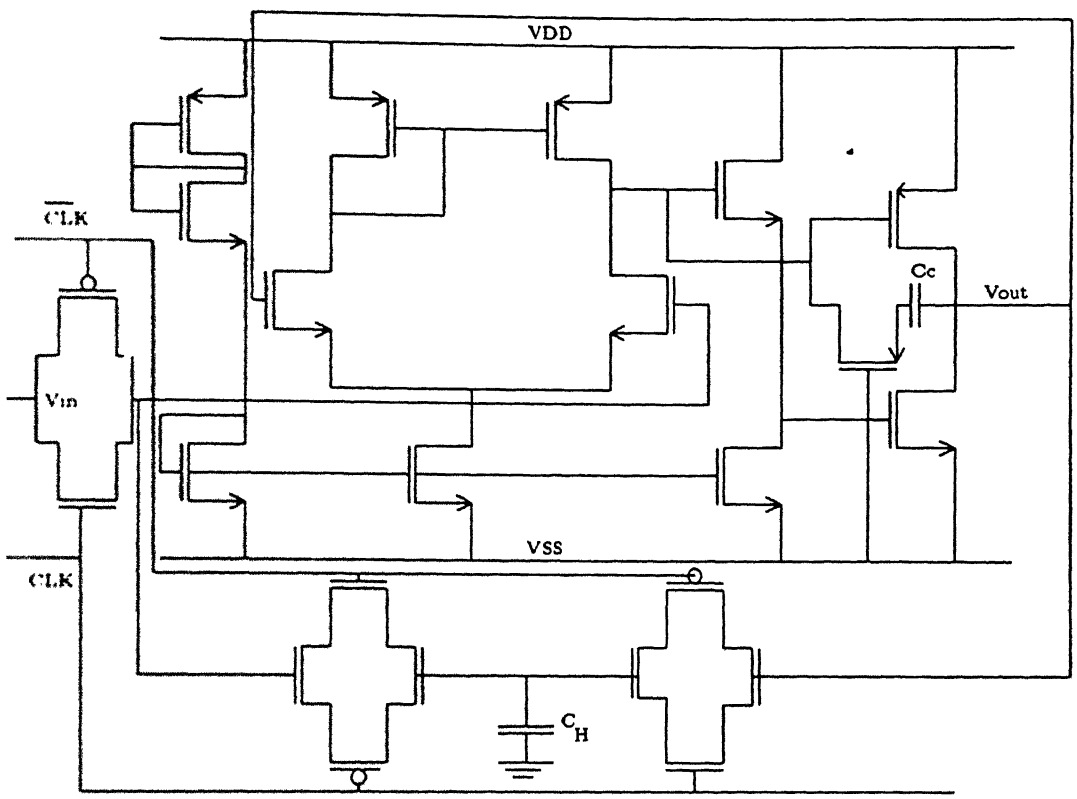


Figure 4.10: S & H circuit with opamp scheme 2

Chapter 5

EVALUATION OF PERFORMANCE

From the input performance specifications, KANSYS produces a sized transistor level circuit schematic in the form of a SPICE file. This particular form of output has been chosen for the ease of simulation for the user. Detailed circuit simulation for performance shows that the worst case design can be designed within an error of 20%. However the error for the specifications which are the critical ones for circuit behaviour is limited to 10%.

We consider sets of closely related specifications for demonstrating the design style selection and translation process in KANSYS for some of the circuits synthesized. A change in the input specifications can result not only in different sizing but in an entirely different topology as well. We present the sized transistor schematics and the SPICE files generated by KANSYS for each set of performance specifications for some of the circuits which are the most useful in demonstrating the design style selection and translation process, as also the results in a tabular form.

5.1 Bias Circuits

Three basic topologies are designed for the Bias Circuits. The bias chain which provides biasing arrangement in the differential output operational amplifier is not

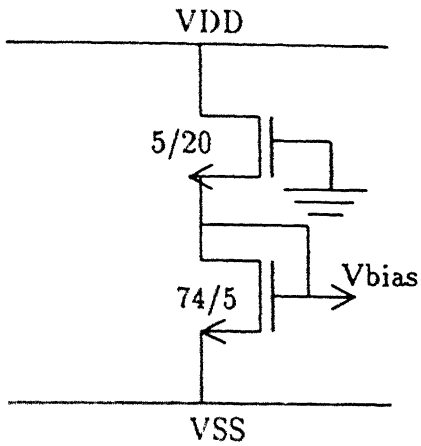


Figure 5.1: Bias Circuit 1

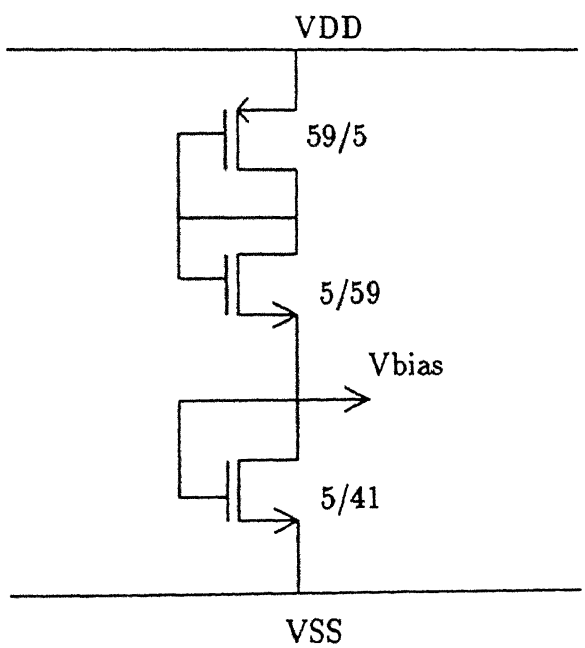


Figure 5.2: Bias Circuit 2

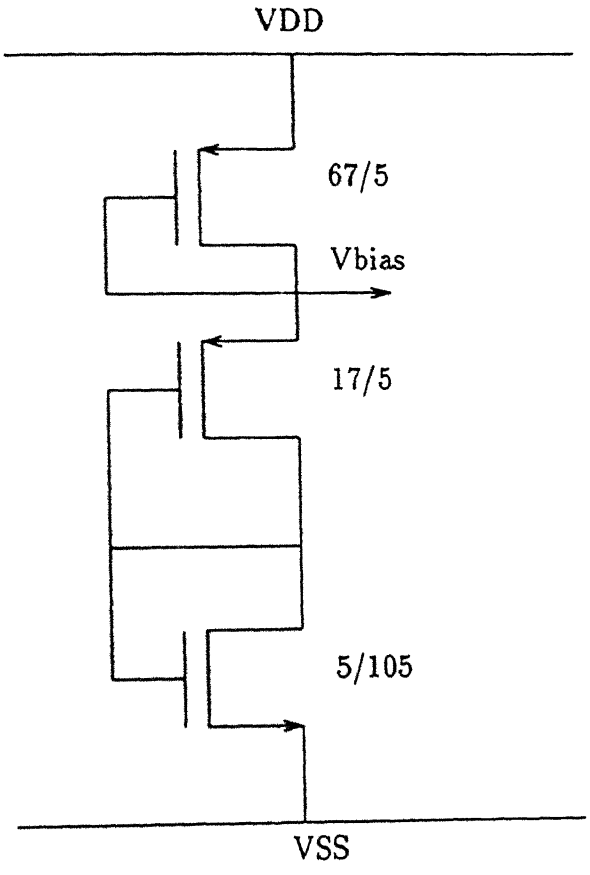


Figure 5.3: Bias circuit 3

considered here as it is not reused in any other circuit and is specific to only scheme 5 of operational amplifier.

Parameter	Bias Circuit 1		Bias circuit 2		Bias Circuit 3	
	Spec.	Spice sim.	Spec.	Spice sim.	Spec.	Spice sim.
Bias voltage(v)	-3.5	-3.48	-0.5	-0.6	3.5	3.47
Current(μA)	40	48	40	33	40	46.7

The sized transistor schematics for all the three schemes are shown in Figs. 5.1, 5.2, 5.3. The SPICE files are present in the appendix.

5.2 Level Shifter

Two basic topologies are designed for the level shifter block. If the output voltage required is less than the input voltage, the first topology is chosen, else the second topology is chosen.

Parameter	Level shifter 1		Level Shifter 2	
	Spec.	Spice sim.	Spec.	Spice sim.
Input voltage(v)	4	4	-1	-1
Output voltage(v)	1	0.97	3	2.985
Current(μA)	40	46.7	40	47.3

The sized transistor schematics for both the schemes are shown in Figs. 5.4 and 5.5. The SPICE files are present in the appendix.

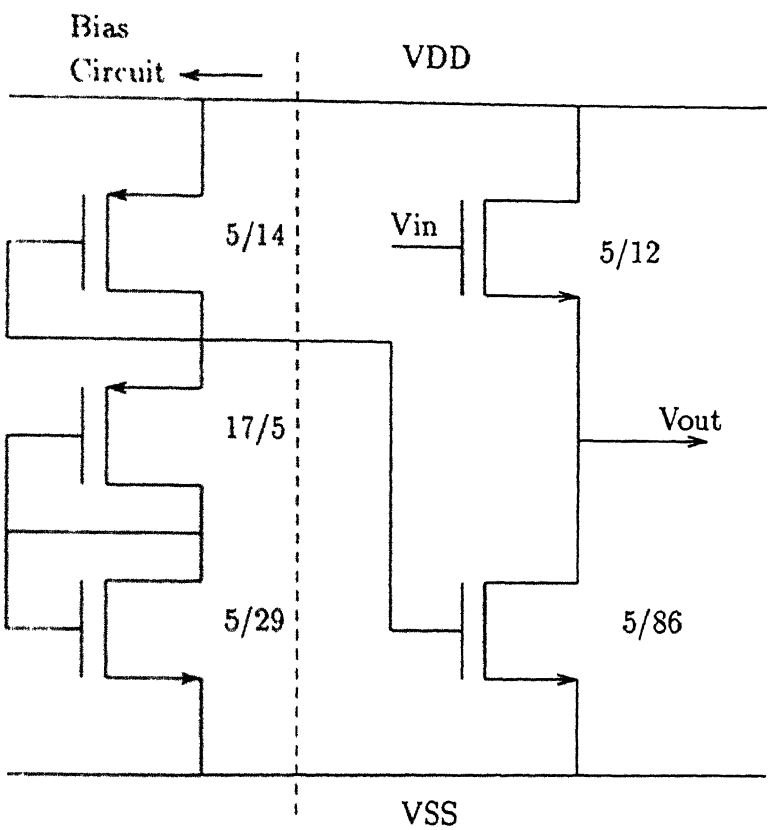


Figure 5.4: Level Shifter 1

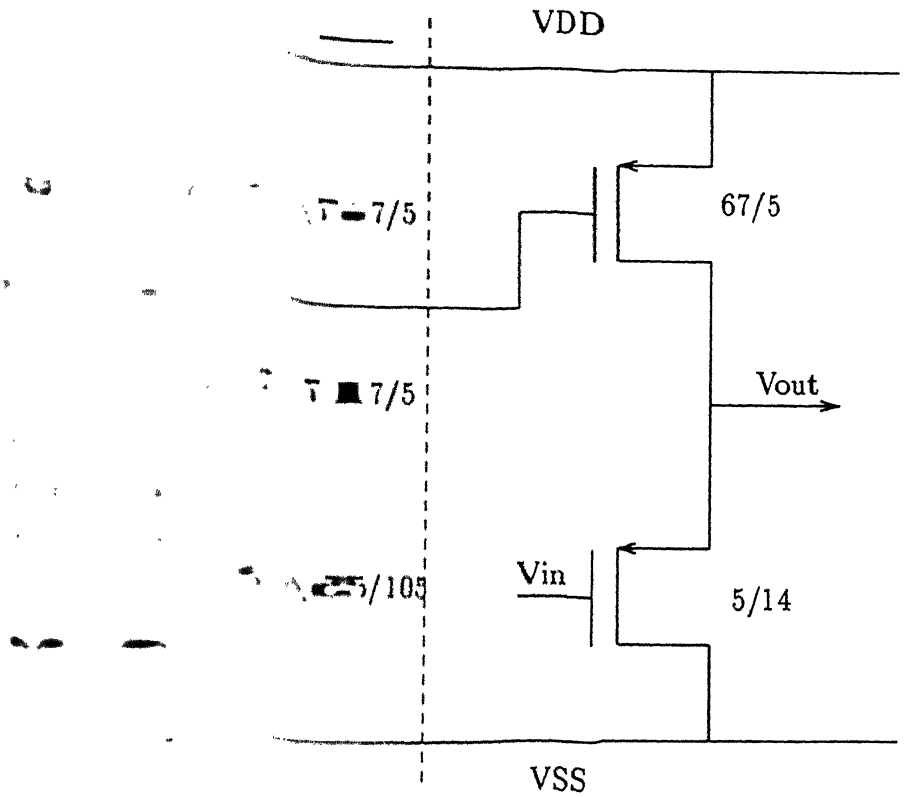


Figure 5.5: Level Shifter 2

5.3 Gain stage

Only a single topology is considered for this case.

Parameter	Gain Stage	
	Spec.	Spice sim.
Gain(db)	25	25.56
Current(μA)	40	51
Capacitor(pF)	20	20

The sized transistor schematic is shown in Fig. 5.6.

5.4 Current mirror

We do not discuss the results of current mirror as both the topologies are incorporated in the two schemes for the differential amplifier.

5.5 Differential Amplifier

Two basic topologies are used in the form of interconnection of blocks. However more than two transistor level topologies are created as different bias circuits and current mirror load combinations are possible.

Parameter	Scheme 1		Scheme 2	
	Spec.	Spice sim.	Spec.	Spice sim.
Gain(db)	45	44.8	80	80.9
CMRR(db)	45	50	80	90
Capacitor(pF)	20	20	12	12
Frequency(Mhz)	2	2.1	2	2
Current(μA)	40	52.5	40	37

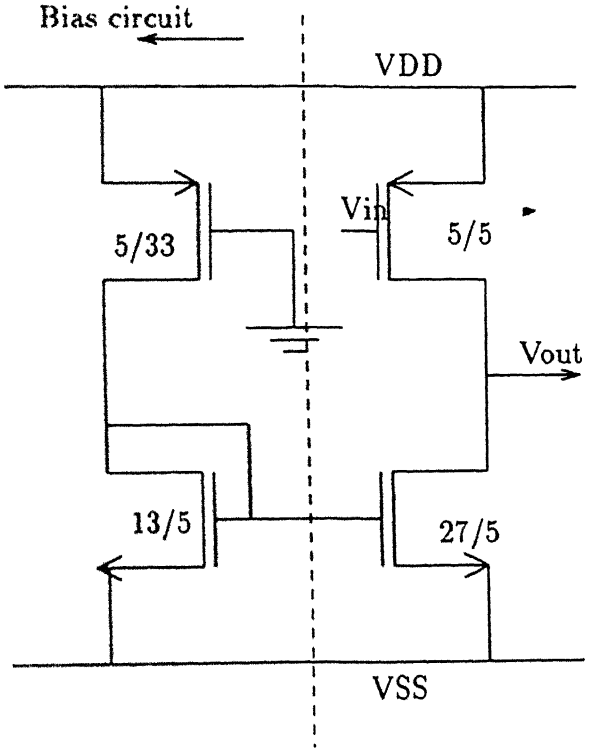


Figure 5.6: Sized Gain stage

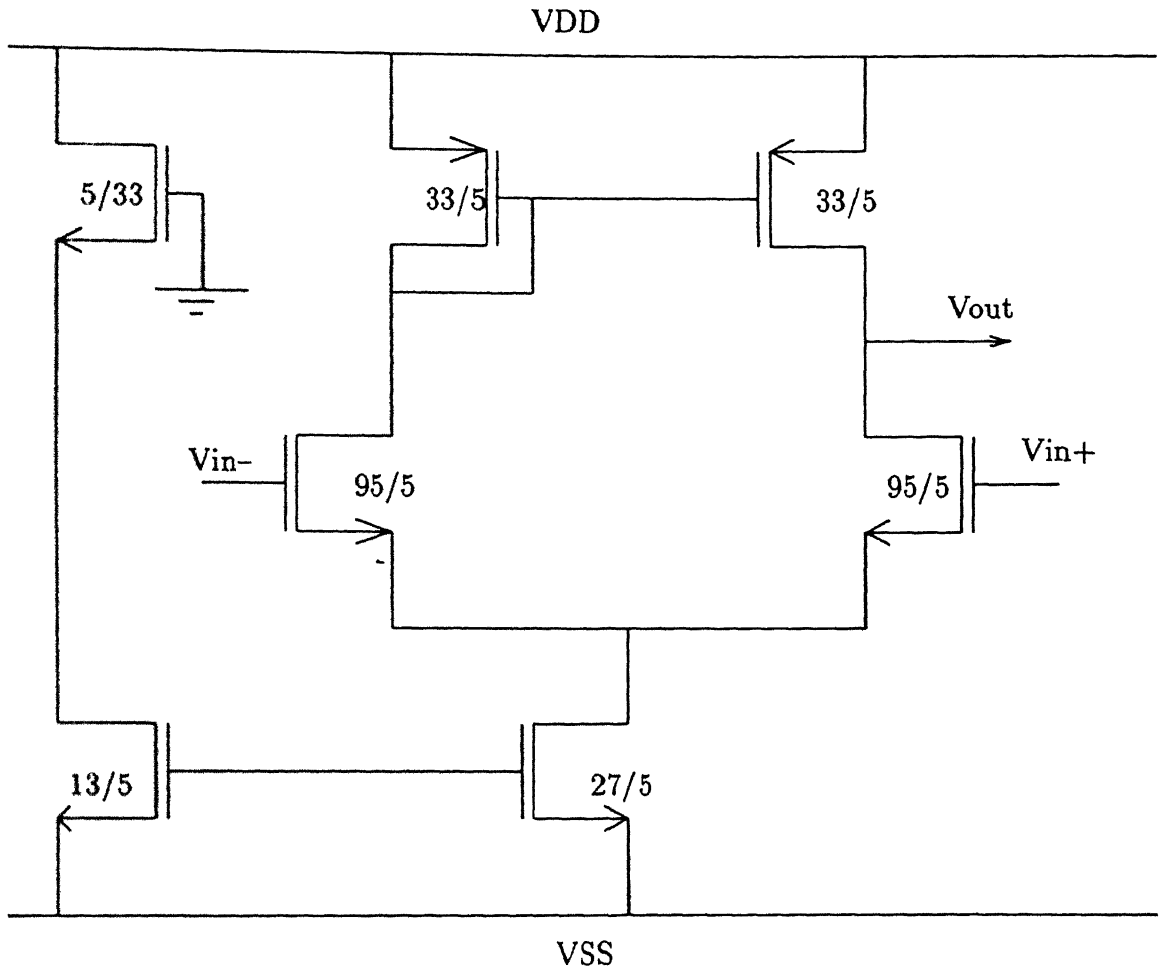


Figure 5.7: Sized simple differential amplifier

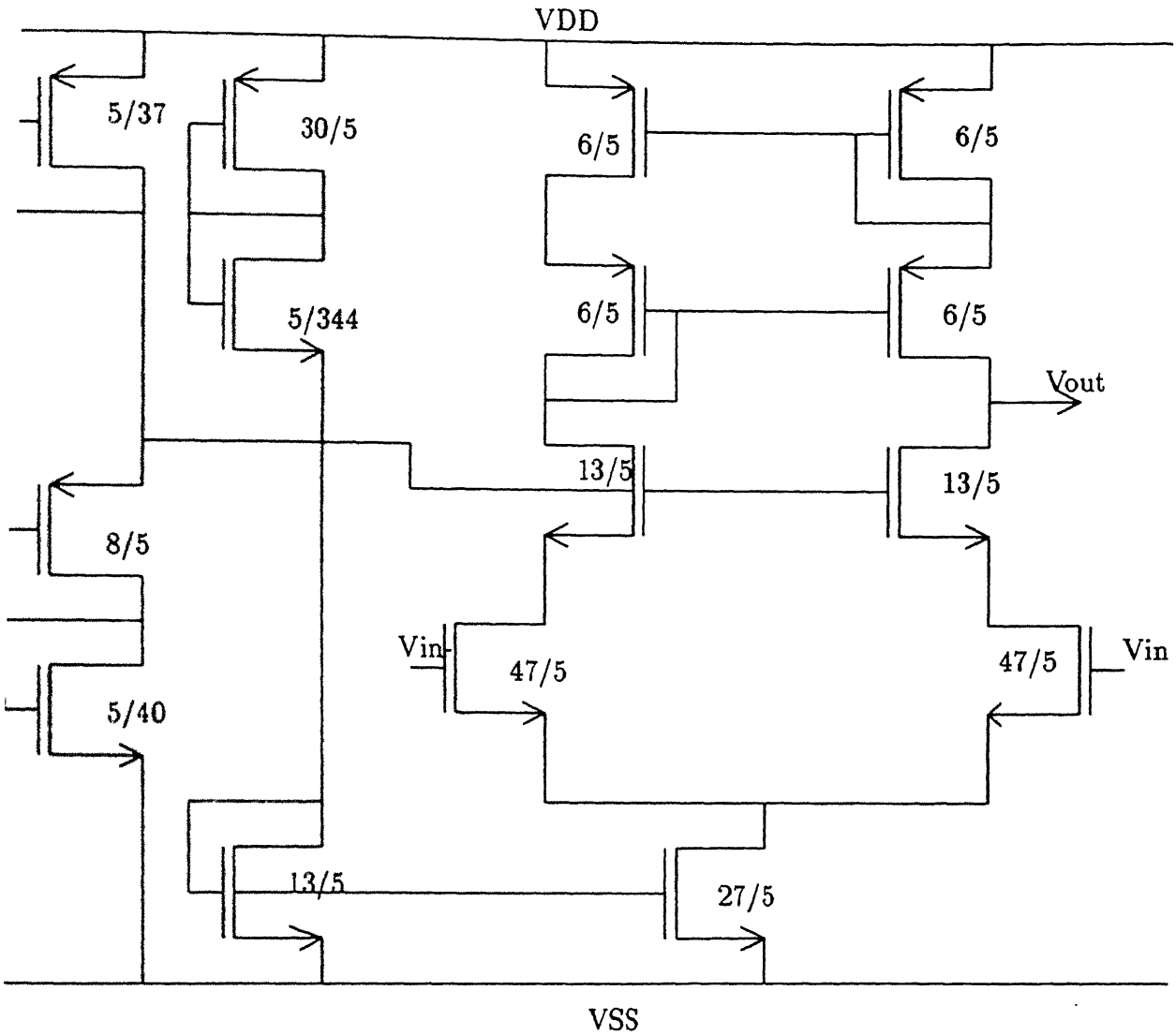


Figure 5.8: Sized cascode differential amplifier

The sized transistor schematics are shown in Figs 5.7 and 5.8.

.6 Operational Amplifier

ve basic topologies are used in the form of interconnection of blocks. However any more transistor level topologies are possible because of the hierarchical deimposition of design styles. High performance opamps, especially scheme 3, have een automated for limited ranges of values. Schemes 4 and 5 have limited hierarchy id therefore not many transistor level topologies are possible for these schemes. ive sets of closely related specifications are considered to illustrate the selection iechanism.

Parameter	Scheme 1		Scheme 2		Scheme 3		Scheme 4		Scheme 5	
	Spec.	Spice sim.	Spec.	Spice sim.	Spec.	Spice sim.	Spec.	Spice sim.	Spec.	Spice sim.
Gain(db)	75	80.9	75	83.7	110	124	80	85.4	80	77.4
CMRR(db)	80	87	80	90	110	130	80	92	80	84
Slew rate(v/μs)	4	5.2	4	5.2	4	3.2	4	4.66	3	3.8
Frequency(Mhz)	3	3.4	3	3.4	3	3.55	4	4.7	3	3.1
Capacitor(pF)	15	15	15	15	12	12	15	15	20	20
Phase Margin(o)	60	78	60	84	60	67	60	90	60	90

The sized transistor schematics are shown in Figs. 5.9 to 5.13.

5.7 Sample and hold circuit

The two topologies considered here are based on the different schemes used in the opamp. The schemes of the opamp that are used are Scheme 2 and Scheme 4. Here since the only two specifications we consider are capacitance and unity gain frequency which are not in the form of requirements on performance, SPICE simulation results are not shown in the table. However using a sinusoidal input waveform

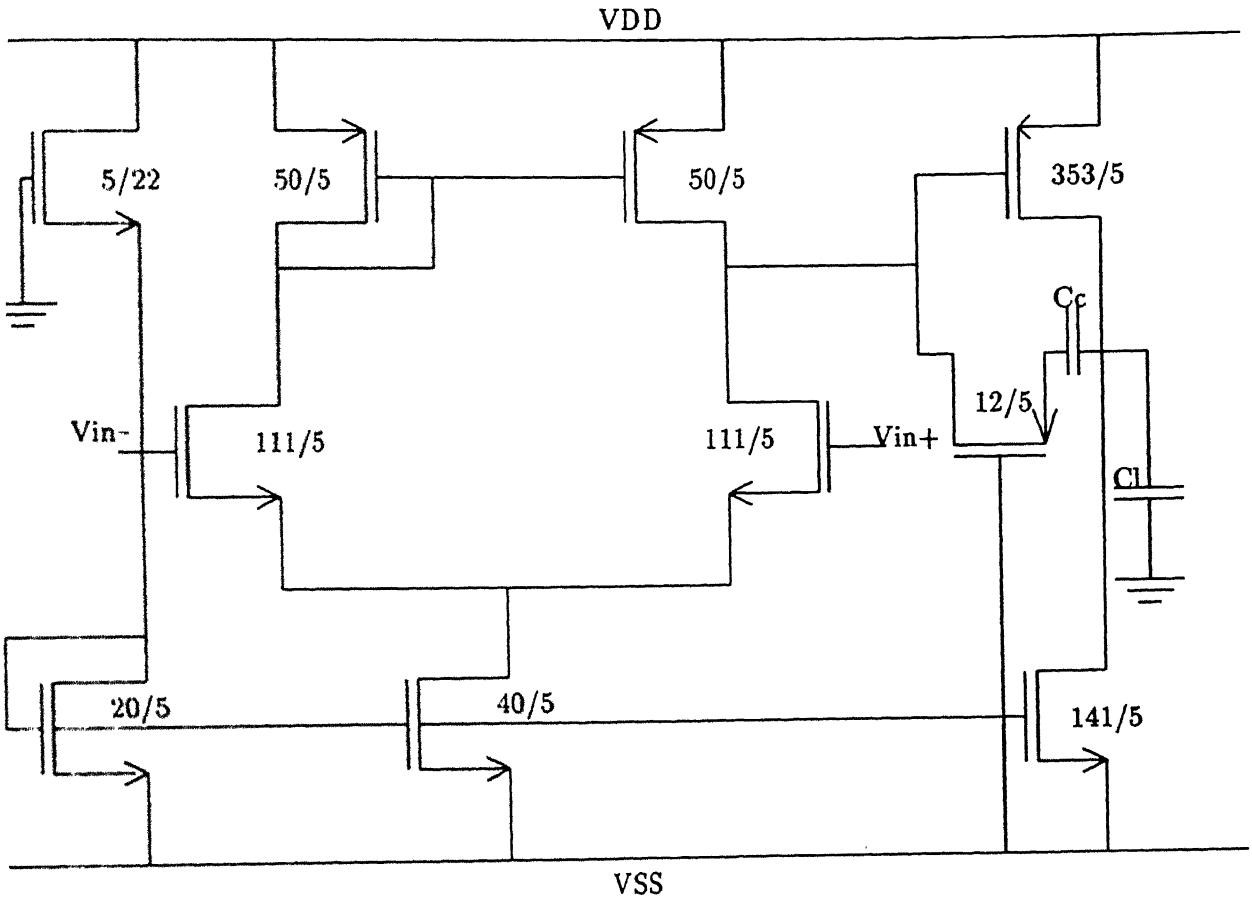


Figure 5.9: Sized scheme 1

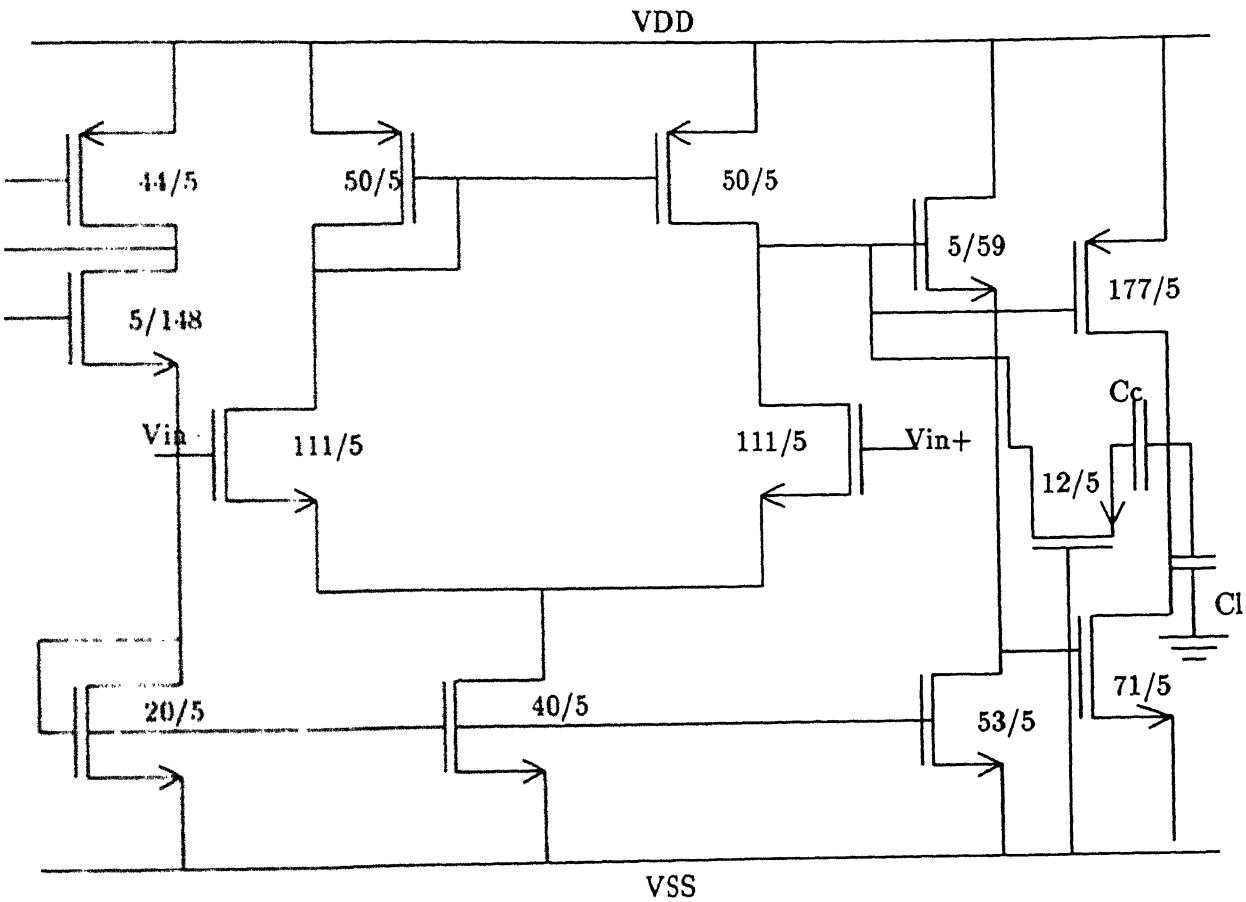


Figure 5.10: Sized scheme 2

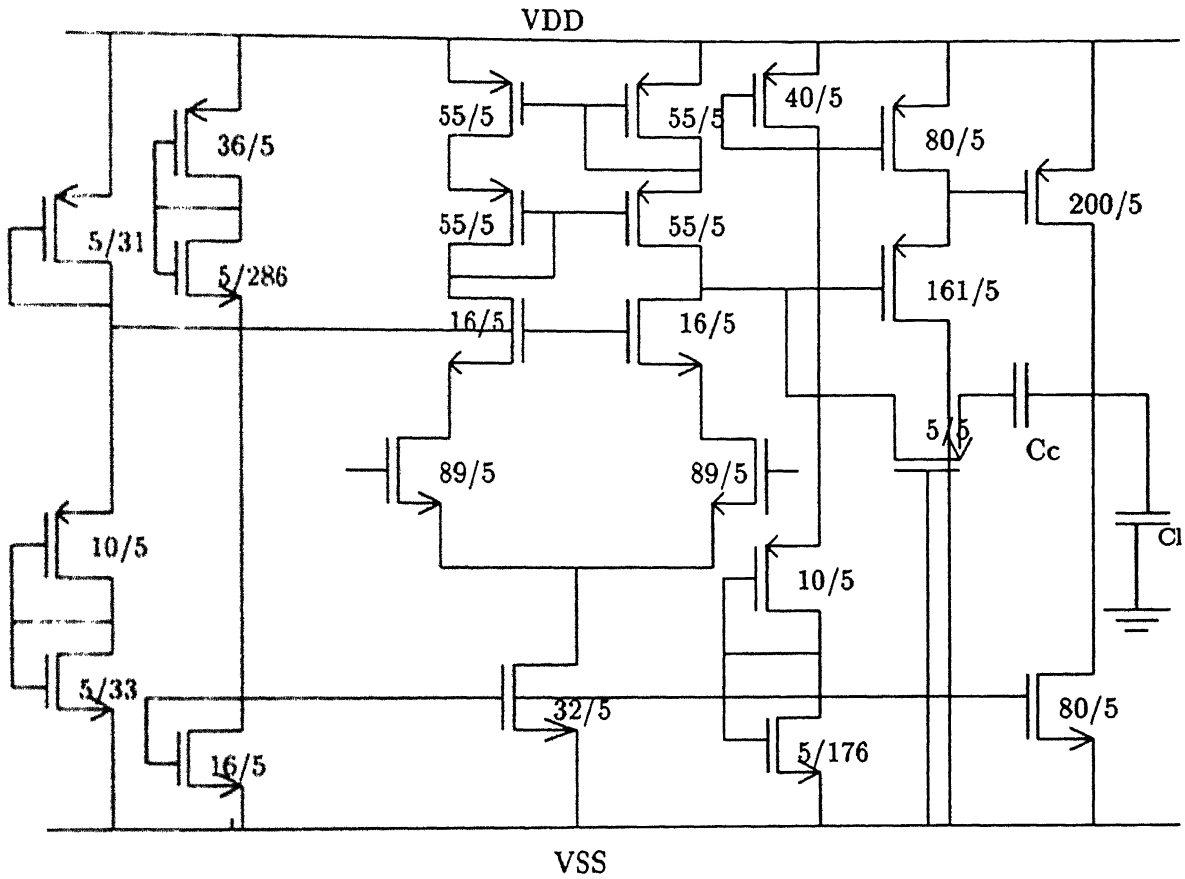


Figure 5.11: Sized scheme 3

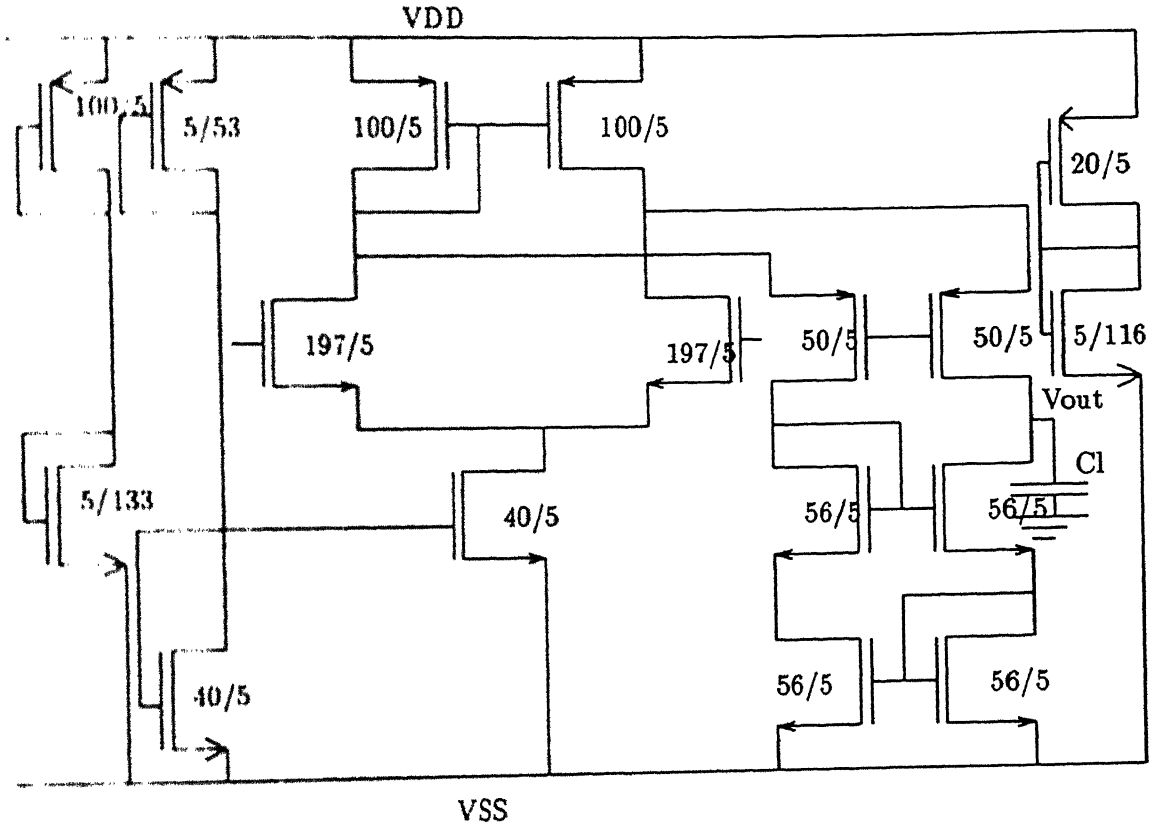


Figure 5.12: Sized scheme 4

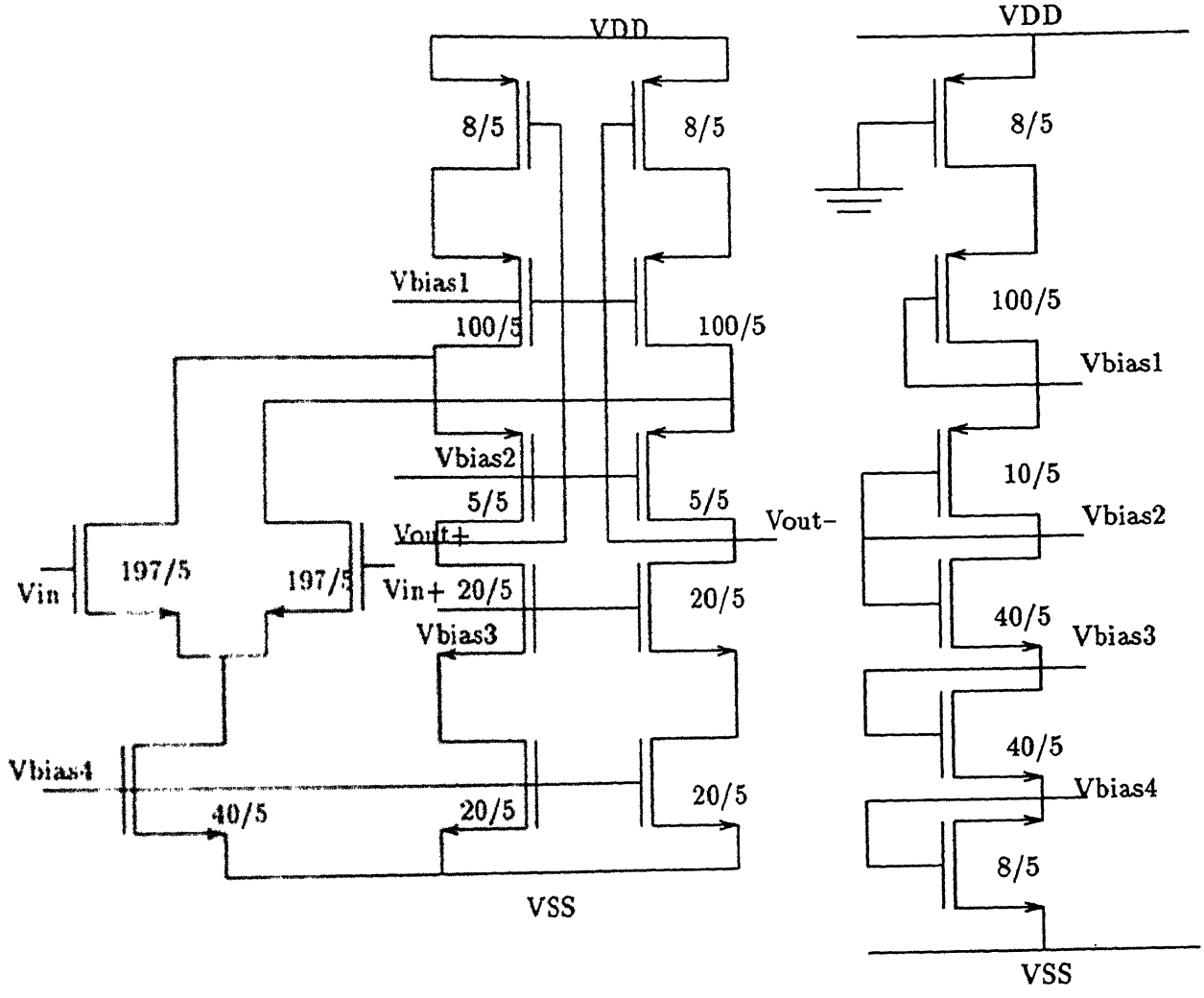


Figure 5.13: Sized scheme 5

and periodic sampling pulse, we verify by detailed simulation that the circuit acts as a good sample and hold circuit.

Parameter	S & H circuit 1	S & H circuit 2
	Specifications	Specifications
Capacitor(pF)	20	20
Frequency(Mhz)	4	3

The sized transistor schematics are not shown as a large part of the circuit is common with the opamp. The SPICE files are however present in the appendix.

5.8 Digital to Analog converter

The design of Digital to Analog converter takes as performance specifications the input bits only. It is implemented on a fixed topology scheme. Detailed simulation shows that output analog voltage is produced to an accuracy of 2mv which is less than the LSB which is ~8mv.

The sized transistor schematic is not shown as a large part of the circuit is common with the opamp. The SPICE file is however present in the appendix.

5.9 Preparation of IC layout:-

NELSIS IC design system[20] can be used for the preparation of IC layout of the synthesized circuits. Parasitic capacitance extraction from the layouts and subsequent simulation by SPICE (as NELSIS does not support analog circuit simulation) can be done to verify the correctness of the design. We present here an example case for opamp scheme 1 with the following set of user specifications:

1. Low frequency gain, $A_o = 70db$
2. Unity gain frequency, $f_o = 2Mhz$

3. Slew rate, SR = 5v/μs

4. Common mode rejection ratio, CMRR = 80db

5. Phase Margin, ϕM =60°

6. Load impedance, C_l = 10pf

and the following process specifications:

1. Transconductance factor = 30μA/v^2 for NMOS devices and 12μA/v^2 for PMOS device.

2. Threshold voltage V_T = 1.2v for NMOS devices and -1v for PMOS devices.

3. Channel length modulation, $\lambda = 0.03\text{v}^{-1}$

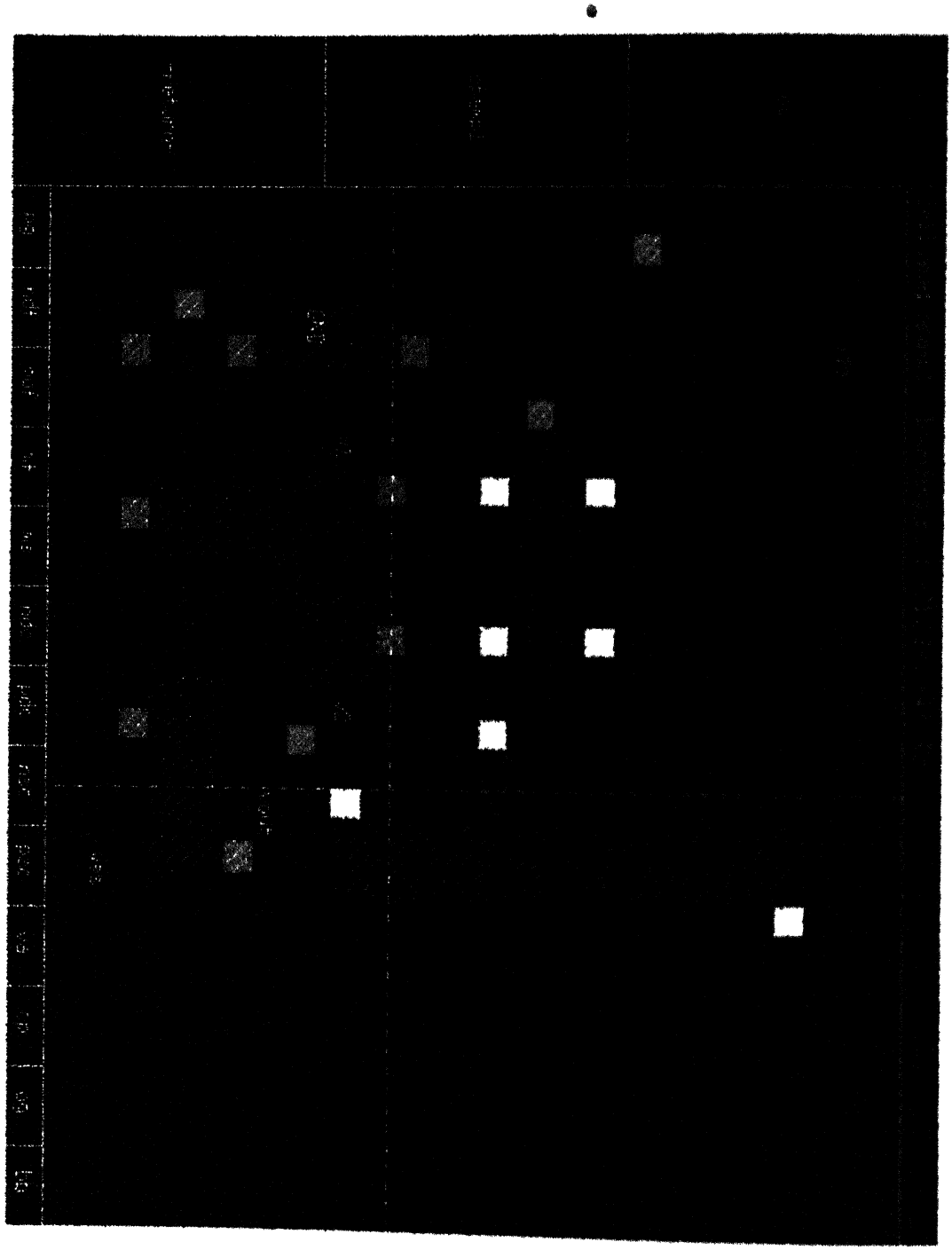
The layout prepared using the layout editor "Xdali" of the IC design system and the SPICE file "OPAMP CIRCUIT 1", prepared after adding the parasitic capacitances are attached. Simulation shows that for the circuit synthesized, A_o = 76.25db, f_o = 2.55Mhz, SR = 5.6v/μs, CMRR = 88db, ϕM = 78°, C_l =10pf. Also systematic offset voltage is $1.38/10^{76.25/20}$ = 0.2mv.

This demonstrates the feasibility of the circuits synthesized using KANSYS for the actual fabrication of IC's.

OPAMP CIRCUIT 1

```
*simple two stage with parasitic capacitances extracted from layout
M0 3 2 1 1 mod1 w=27u l=5u
M1 5 4 3 3 mod1 w=33u l=5u
M2 6 7 3 3 mod1 w=33u l=5u
M3 5 5 8 8 mod2 w=33u l=5u
M4 6 5 8 8 mod2 w=33u l=5u
M5 8 0 2 2 mod1 w=5u l=33u
M6 2 2 1 1 mod1 w=13u l=5u
M7 10 6 8 8 mod2 w=157u l=5u
M8 10 2 1 1 mod1 w=63u l=5u
M9 6 1 9 9 mod2 w=5u l=5u
vdd 8 0 5
vss 0 1 5
cl1 10 0 10.87p
cc 9 10 10.00p
*parasitic capacitances as obtained from IC layout
c1 1 0 0.722p
c2 3 0 0.559p
c3 4 0 0.005p
c4 7 0 0.005p
c5 5 0 0.348p
c6 6 0 0.4p
c7 2 0 0.163p
c8 8 0 1.16p
.model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
.model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
e1 0 4 7 0 1
v1 7 0 ac 0.5
**v2 4 0 pwl(0 0 100ns 0 100ns 5 600ns 5)
.ac dec 10 1 10meg
**.tran 1ns 0.6us
**.op
.end
```

ame: sandep, Date: Sun Feb 19 21:46:53 IST 1995, Paintraw output(CC/IITK



Chapter 6

CONCLUSION AND SCOPE FOR FUTURE WORK

A framework to support behaviour to structure synthesis for analog circuits has been implemented. The synthesis starts from a set of system level specifications. KANSYS selects the most promising circuit in its database based on the design requirements implied by the specifications. Implementation of mechanisms for managing the hierarchy(together with some design knowledge of the flattened circuit), the design style selection and translation have been described. Detailed circuit simulation using SPICE and parasitics extraction from IC layouts using NELSIS shows that KANSYS produces practical circuit configurations for actual IC fabrication. Using the framework, the entire synthesis process is very fast and the program can be used by system engineers who are inexperienced in circuit design. They simply specify their design requirements and in a few seconds, with no further interactive details being asked, the system offers one or more of the designs that meet functional specifications., except for the most stringent designs.

KANSYS has been written in ANSI C and is compatible with UNIX version 9.0.

SUGGESTION FOR FUTURE WORK

The framework described here can be extended to a silicon compilation system which supports the automated translation of behavioural specifications to IC masks. Also standard tools for layout of analog cells can be used which take KANSYS synthesized circuits and automatically reduce them to masks.

Currently since KANSYS supports the synthesis of analog circuits upto the level of a macrocell, it can be upgraded for the synthesis of a system or a macromodule. Among the other possibilities, which require only slight modification, are (i) To interface KANSYS with some numerical optimization tool to further fine tune the device sizes based on specific goals, say performance enhancement. One such tool is DELIGHT.SPICE[11]. (ii) To interface KANSYS with NELSIS to produce IC layouts automatically, using the ldmc language provided with NELSIS.

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Bias circuit 1

```
M0 3 0 2 2 mod1 w=5u l=20u
M1 2 2 1 1 mod1 w=74u l=5u
vdd 3 0 5
vss 0 1 5
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
 op
 end
```

Bias circuit 2

```
M0 3 3 4 4 mod2 w=59u l=5u
M1 3 3 2 2 mod1 w=5u l=59u
M2 2 2 1 1 mod1 w=5u l=41u
vdd 4 0 5
vss 0 1 5
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
 op
 end
```

Bias circuit 3

```
M0 3 3 4 4 mod2 w=67u l=5u
M1 2 2 3 3 mod2 w=17u l=5u
M2 2 2 1 1 mod1 w=5u l=105u
vdd 4 0 5
vss 0 1 5
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
 op
 end
```

Level shifter 1

```
*with output dc voltage less than input dc voltage
M0 5 4 3 3 mod1 w=5u l=12u
M1 3 2 1 1 mod1 w=5u l=86u
M2 2 2 5 5 mod2 w=5u l=14u
M3 6 6 2 2 mod2 w=17u l=5u
M4 6 6 1 1 mod1 w=5u l=29u
vdd 5 0 5
vss 0 1 5
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
vin 4 0 4 00
 op
 end
```

Level Shifter 2

```
*with output dc voltage more than input dc voltage
M0 3 4 5 5 mod2 w=67u l=5u
M1 1 2 3 3 mod2 w=5u l=14u
M2 4 4 5 5 mod2 w=67u l=5u
M3 6 6 4 4 mod2 w=17u l=5u
M4 6 6 1 1 mod1 w=5u l=105u
vdd 5 0 5
vss 0 1 5
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
vin 2 0 -1.00
 op
 end
```

Differential Amplifier

```
*with sumple current mirror
M0 2 1 8 8 mod1 w=27u l=5u
M1 4 3 2 2 mod1 w=95u l=5u
M2 6 5 2 2 mod1 w=95u l=5u
M3 4 4 7 7 mod2 w=33u l=5u
M4 6 4 7 7 mod2 w=33u l=5u
M5 7 0 1 1 mod1 w=5u l=33u
M6 1 1 8 8 mod1 w=13u l=5u
vdd 7 0 5
vss 0 8 5
cl1 6 0 20 00p
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
e1 0 3 5 0 1
v1 5 0 ac 0 5
 ac dec 10 1 10meg
 end
```

Differential Amplifier

```
*with cascode load in the differential stage
M0 2 1 12 12 mod1 w=27u l=5u
M1 5 3 2 2 mod1 w=47u l=5u
M2 6 4 2 2 mod1 w=47u l=5u
M3 9 10 11 11 mod2 w=6u l=5u
M4 10 10 11 11 mod2 w=6u l=5u
M5 7 7 9 9 mod2 w=6u l=5u
M6 8 7 10 10 mod2 w=6u l=5u
M7 7 14 5 5 mod1 w=13u l=5u
M8 8 14 6 6 mod1 w=13u l=5u
M9 13 13 11 11 mod2 w=30u l=5u
M10 13 13 1 1 mod1 w=5u l=344u
M11 1 1 12 12 mod1 w=13u l=5u
M12 14 14 11 11 mod2 w=5u l=37u
M13 15 15 14 14 mod2 w=8u l=5u
M14 15 15 12 12 mod1 w=5u l=40u
vdd 11 0 5
vss 0 12 5
cl1 8 0 12.00p
.model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
e1 0 3 4 0 1
v1 4 0 ac 0.5
.ac dec 10 1 10meg
.end
```

OPAMP CIRCUIT 1

```
*simple two stage
M0 3 2 1 1 mod1 w=40u l=5u
M1 5 4 3 3 mod1 w=111u l=5u
M2 6 7 3 3 mod1 w=111u l=5u
M3 5 5 8 8 mod2 w=50u l=5u
M4 6 5 8 8 mod2 w=50u l=5u
M5 8 0 2 2 mod1 w=5u l=22u
M6 2 2 1 1 mod1 w=20u l=5u
M7 10 6 8 8 mod2 w=353u l=5u
M8 10 2 1 1 mod1 w=141u l=5u
M9 6 1 9 9 mod2 w=12u l=5u
vdd 8 0 5
vss 0 1 5
cl1 10 0 15 00p
cc 9 10 15 00p
 model mod1 nmos(vto=1 20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
el 0 4 7 0 1
vl 7 0 ac 0.5
 ac dec 10 1 10meg
 end
```

OPAMP CIRCUIT 2

```
*Two stage with level shifter
M0 3 2 1 1 mod1 w=40u l=5u
M1 5 4 3 3 mod1 w=111u l=5u
M2 6 7 3 3 mod1 w=111u l=5u
M3 5 5 8 8 mod2 w=50u l=5u
M4 6 5 8 8 mod2 w=50u l=5u
M5 9 9 8 8 mod2 w=44u l=5u
M6 9 9 2 2 mod1 w=5u l=148u
M7 2 2 1 1 mod1 w=20u l=5u
M8 12 6 8 8 mod2 w=177u l=5u
M9 12 10 1 1 mod1 w=71u l=5u
M10 6 1 11 11 mod2 w=12u l=5u
M11 8 6 10 10 mod1 w=5u l=59u
M12 10 2 1 1 mod1 w=53u l=5u
vdd 8 0 5
vss 0 1 5
cl1 12 0 15 00p
cc 11 12 15 00p
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1 00,lambda=0.03,kp=24u)
e1 0 4 7 0 1
v1 7 0 ac 0.5
 ac dec 10 1 10meg
 end
```

OPAMP CIRCUIT 3

```
*Two stage with cascode load in differential amplifier
M0 2 1 12 12 mod1 w=32u l=5u
M1 5 3 2 2 mod1 w=89u l=5u
M2 6 4 2 2 mod1 w=89u l=5u
M3 9 10 11 11 mod2 w=55u l=5u
M4 10 10 11 11 mod2 w=55u l=5u
M5 7 9 9 mod2 w=55u l=5u
M6 8 7 10 10 mod2 w=55u l=5u
M7 7 14 5 5 mod1 w=16u l=5u
M8 8 14 6 6 mod1 w=16u l=5u
M9 13 13 11 11 mod2 w=36u l=5u
M10 13 13 1 1 mod1 w=5u l=286u
M11 1 1 12 12 mod1 w=16u l=5u
M12 14 14 11 11 mod2 w=5u l=31u
M13 15 15 14 14 mod2 w=10u l=5u
M14 15 15 12 12 mod1 w=5u l=33u
M15 12 8 18 18 mod2 w=161u l=5u
M16 18 17 11 11 mod2 w=80u l=5u
M17 17 17 11 11 mod2 w=40u l=5u
M18 16 16 17 17 mod2 w=10u l=5u
M19 16 16 12 12 mod1 w=5u l=176u
M20 20 18 11 11 mod2 w=200u l=5u
M21 20 1 12 12 mod1 w=80u l=5u
M22 8 12 19 19 mod2 w=5u l=5u
vdd 11 0 5
vss 0 12 5
cl1 20 0 12 00p
cc 19 20 12 00p
.model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
.model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
e1 0 3 4 0 1
v1 4 0 ac 0.5
.ac dec 10 1 10meg
.end
```

OPAMP CIRCUIT 4

```
*Wideband folded cascode cmos opamp
M0 2 2 8 8 mod2 w= 5u l= 53u
M1 2 2 1 1 mod1 w= 40u l= 5u
M2 9 9 1 1 mod1 w= 5u l=133u
M3 9 9 8 8 mod2 w= 100u l=5u
M4 10 10 1 1 mod1 w= 5u l= 116u
M5 10 10 8 8 mod2 w=20u l=5u
M6 5 4 3 3 mod1 w= 197u l=5u
M7 5 9 8 8 mod2 w= 100u l=5u
M8 3 2 1 1 mod1 w= 40u l=5u
M9 6 7 3 3 mod1 w=197u l=5u
M10 11 10 5 5 mod2 w= 50u l= 5u
M11 6 9 8 8 mod2 w=100u l=5u
M12 13 14 1 1 mod1 w=56u l=5u
M13 11 11 13 13 mod1 w=56u l=5u
M14 12 10 6 6 mod2 w=50u l=5u
M15 14 14 1 1 mod1 w= 56u l=5u
M16 12 11 14 14 mod1 w=56u l=5u
vdd 8 0 5
vss 0 1 5
cl1 12 0 15 00p
 model mod1 nmos(vto= 1 20,lambda=0 03,kp=60u)
 model mod2 pmos(vto=-1 00,lambda=0 03,kp=24u)
e1 0 4 7 0 1
v1 7 0 ac 0 5
 ac dec 10 1 10meg
 end
```

OPAMP CIRCUIT 5

```
*Differential output cmos opamp
M1 5 4 3 3 mod1 w=19u l=5u
M1 6 2 3 3 mod1 w=19u l=5u
M2 9 10 11 11 mod2 w=8u l=5u
M3 9 13 11 11 mod2 w=8u l=5u
M4 5 8 9 9 mod2 w=100u l=5u
M5 6 8 9 9 mod2 w=100u l=5u
M6 10 12 5 5 mod2 w=5u l=5u
M7 13 12 6 6 mod2 w=5u l=5u
M8 10 14 15 15 mod1 w=20u l=5u
M9 13 14 16 16 mod1 w=20u l=5u
M10 15 2 1 1 mod1 w=20u l=5u
M11 16 2 1 1 mod1 w=20u l=5u
M12 3 2 1 1 mod1 w=40u l=5u
M13 17 0 11 11 mod2 w=8u l=5u
M14 8 8 17 17 mod2 w=100u l=5u
M15 12 12 8 8 mod2 w=10u l=5u
M16 14 14 2 2 mod1 w=40u l=5u
M17 2 2 1 1 mod1 w=40u l=5u
M18 12 12 14 14 mod1 w=8u l=5u
vdd 11 0 5
vss 0 1 5
cl1 10 0 20.00p
cl2 13 0 20.00p
.model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
.model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
c1 0 4 .01
v1 7 0 ac 0.5
.ac dec 10 1 10meg
.end
```

Sample and hold circuit

```
*with wideband folded cascode opamp
M0 2 2 8 8 mod2 w=5u l=80u
M1 2 2 1 1 mod1 w=27u l=5u
M2 9 9 1 1 mod1 w=5u l=200u
M3 9 9 8 8 mod2 w=67u l=5u
M4 10 10 1 1 mod1 w=5u l=173u
M5 10 10 8 8 mod2 w=12u l=5u
M6 5 4 3 3 mod1 w=526u l=5u
M7 5 9 8 8 mod2 w=67u l=5u
M8 3 2 1 1 mod1 w=27u l=5u
M9 6 7 3 3 mod1 w=526u l=5u
M10 11 10 5 5 mod2 w=33u l=5u
M11 6 9 8 8 mod2 w=67u l=5u
M12 13 14 1 1 mod1 w=37u l=5u
M13 11 11 13 13 mod1 w=37u l=5u
M14 12 10 6 6 mod2 w=33u l=5u
M15 14 14 1 1 mod1 w=37u l=5u
M16 12 11 14 14 mod1 w=37u l=5u
M17 7 17 16 16 mod2 w=5u l=5u
M18 16 18 7 7 mod1 w=5u l=5u
M19 19 17 7 7 mod1 w=5u l=5u
M20 7 18 19 19 mod2 w=5u l=5u
M21 12 17 19 19 mod2 w=13u l=5u
M22 19 18 12 12 mod1 w=33u l=5u
vdd 8 0 5
vss 0 1 5
cll 19 0 20 00p
 model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
 model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
v1 4 12 0
vin 16 0 sin(0 5 250khz)
vclkb 17 0 dc 0 pulse(-5 5 2us 0 0 15.5us 17.5us)
e1 0 18 17 0 1
 tran 10ns 30us
 end
```

Sample and hold circuit

```
*with two stage(level shifter included) opamp
M0 3 2 1 1 mod1 w=27u l=5u
M1 5 4 3 3 mod1 w=296u l=5u
M2 6 7 3 3 mod1 w=296u l=5u
M3 5 5 8 8 mod2 w=33u l=5u
M4 6 5 8 8 mod2 w=33u l=5u
M5 9 9 8 8 mod2 w=30u l=5u
M6 9 9 2 2 mod1 w=5u l=222u
M7 2 2 1 1 mod1 w=13u l=5u
M8 12 6 8 8 mod2 w=236u l=5u
M9 12 10 1 1 mod1 w=94u l=5u
M10 6 1 11 11 mod2 w=16u l=5u
M11 8 6 10 10 mod1 w=5u l=59u
M12 10 2 1 1 mod1 w=53u l=5u
M13 7 14 13 13 mod2 w=5u l=5u
M14 13 15 7 7 mod1 w=5u l=5u
M15 16 14 7 7 mod1 w=5u l=5u
M16 7 15 16 16 mod2 w=5u l=5u
M17 12 14 16 16 mod2 w=10u l=5u
M18 16 15 12 12 mod1 w=25u l=5u
vdd 8 0 5
vss 0 1 5
cl1 16 0 20.00p
cc 11 12 20.00p
.model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
.model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
v1 4 12 0
vin 13 0 sin(0 5 250khz)
vclkb 14 0 dc 0 pulse(-5 5 2us 0 0 15.5us 17.5us)
e1 0 15 14 0 1
.tran 10ns 30us
.end
```

Digital to Analog converter

```
*with two stage opamp with level shifter
M0 3 2 1 1 mod1 w=27u l=5u
M1 5 4 3 3 mod1 w=33u l=5u
M2 6 7 3 3 mod1 w=33u l=5u
M3 5 5 8 8 mod2 w=33u l=5u
M4 6 5 8 8 mod2 w=33u l=5u
M5 9 9 8 8 mod2 w=30u l=5u
M6 9 9 2 2 mod1 w=5u l=222u
M7 2 2 1 1 mod1 w=13u l=5u
M8 12 6 8 8 mod2 w=79u l=5u
M9 12 10 1 1 mod1 w=31u l=5u
M10 6 1 11 11 mod2 w=5u l=5u
M11 8 6 10 10 mod1 w=5u l=89u
M12 10 2 1 1 mod1 w=35u l=5u
vdd 8 0 5
vss 0 1 5
cl1 12 0 10 00p
cc 11 12 10.00p
.model mod1 nmos(vto=1.20,lambda=0.03,kp=60u)
.model mod2 pmos(vto=-1.00,lambda=0.03,kp=24u)
v0 36 0 5
v1 37 0 5
v2 38 0 5
v3 39 0 5
v4 40 0 5
v5 41 0 5
v6 42 0 5
v7 43 0 5
v8 44 0 5
v9 45 0 5
R0 7 17 10k
R1 17 18 10k
R2 18 19 10k
R3 19 20 10k
R4 20 21 10k
R5 21 22 10k
R6 22 23 10k
R7 23 24 10k
R8 24 25 10k
R9 25 0 20k
R10 7 26 19.5k
R11 17 27 19.5k
R12 18 28 19.5k
R13 19 29 19.5k
R14 20 30 19.5k
R15 21 31 19.5k
R16 22 32 19.5k
R17 23 33 19.5k
R18 24 34 19.5k
R19 25 35 19.5k
R20 16 4 20k
R21 4 12 20k
.subckt switch 1 2 3
M1 1 2 0 0 mod1 w=44u l=5u
M2 1 2 3 3 mod2 w=139u l=5u
```

```
ends
X0 26 36 16 switch
X1 27 37 16 switch
X2 28 38 16 switch
X3 29 39 16 switch
X4 30 40 16 switch
X5 31 41 16 switch
X6 32 42 16 switch
X7 33 43 16 switch
X8 34 44 16 switch
X9 35 45 16 switch
vref 16 0 4.0
.op
.end
```